

Report on Long-Term Testing of the Highland V880 DDG

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**National Ignition Facility Project
Integrated Timing system**

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May 19, 2000

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Abstract

A testing facility for evaluating ITS hardware components has been established in Trailer 3907. In accordance with our acceptance testing of the Highland V880 digital delay generators (DDG), software has been written to allow long-term testing to be performed on the four V880 prototypes (NIF-5000375). Problems and discrepancies discovered through long-term testing have been documented, and a summary of the problems found and the corrective actions taken are presented in this report. For more background information about the National Ignition Facility and the Integrated Timing System, see UCRL-JC-135036.

Purpose

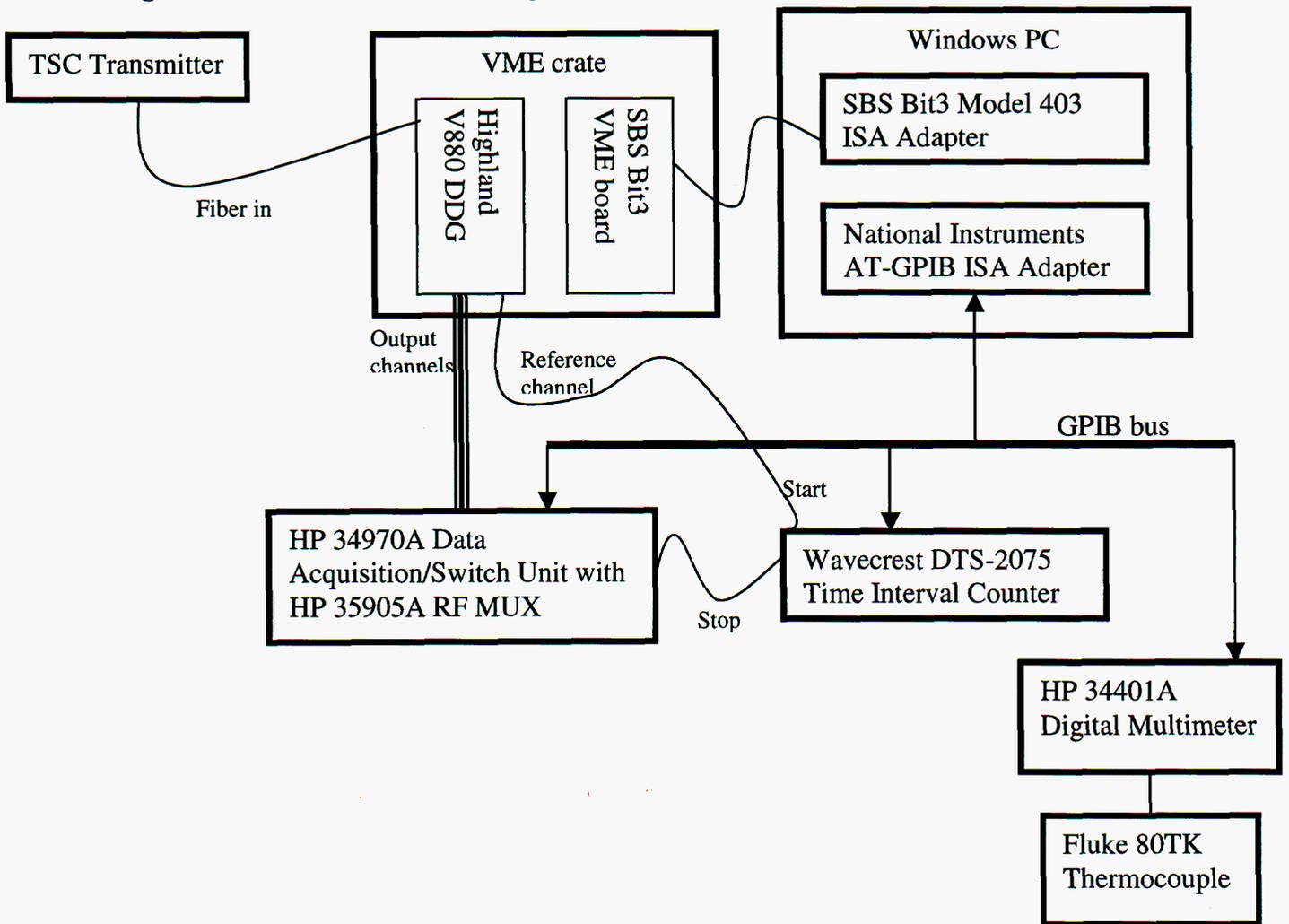
Almost two hundred V880 delay generators are anticipated for use in the National Ignition Facility, therefore the need for a standardized V880 hardware acceptance test facility became evident. The V880 acceptance testing needed to be done independently of the ICCS software development to ensure that acceptance testing would not be complicated by simultaneous ICCS software development. The V880 acceptance test facility can also be used for long-term testing of modules, and is able to detect a wider range of hardware problems than the ICCS software.

Hardware description

As shown in Figure 1, the V880 test setup consists of a PC running Windows 98 that is connected to the V880 DDG VME board, and a time interval counter. The PC uses an ISA to VME bus adapter to communicate with the modules contained within the VME crate, and a GPIB interface to connect to the measurement devices.

In the ITS hardware test facility, the fiber optic output of the Timing Solutions Corporation (TSC) Facility Timing Transmitter (NIF-5000786) provides the master trigger for the timing system. The transmitter is connected through a 1x4 fiber optic splitter (LEA96-2874) to a 9/125-micron single-mode SC/APC input connector (NIF-5001866) on a Highland V880 Digital Delay Generator (DDG) located in a VME crate. The V880 DDG is designed to provide electrical and optical triggers delayed at picosecond accuracies. The trigger channel delays and RMS jitter can be measured using a time interval counter and a reference channel. The DDG trigger channel

Figure 1 ITS Hardware Test Configuration for V880 testing



outputs can be either electrical SMB connectors or optical 50/125-micron multimode ST connectors (NIF-5001867) depending on the module subtype.

A SBS Bit3 Operations Model 403 ISA to VME bus adapter has also been installed in the VME crate. The Bit3 card enables the ITS testing team to use a PC to read and write to the V880 DDG onboard memory registers that are located in its dual port memory. A computer program written in PowerBASIC has been developed by Highland Technology and modified by LLNL for V880 testing purposes. The LLNL modifications allow ITS testing personnel to set trigger channel delays and measure the actual time delays and RMS jitter using a time interval counter. The LLNL additions and changes to the Highland V880 software are documented below.

A Wavecrest DTS-2075 Time Interval Counter is used to measure the trigger delays on each V880 DDG output channel. The reference channel from the V880 is connected to the DTS-2075 as the start trigger, while the trigger channel outputs from the V880 are passed through a 1x8 RF multiplexer and connected to the DTS-2075 as the stop trigger. The time interval between the start and stop trigger is recorded by the time interval counter. The DTS-2075 has been programmed to measure 1000 samples and then display an average time measurement and the RMS jitter.

An IEEE 488.2 compliant GPIB bus is used to interface between the Windows PC and the Wavecrest DTS-2075. In addition, the GPIB bus also allows the PC to control the 1x8 RF multiplexer and a digital multimeter. The RF multiplexer is used to select the trigger channel output to be measured, and the digital multimeter is connected to a digital thermometer, which is used to read the ambient room temperature.

Software description

Highland Technology has written test and diagnostics software for the V880 DDG. This test software enables the ITS test team to easily gain access to the V880 onboard registers through a Bit3 ISA to VME bus adapter. The Highland V880.EXE test program has commands for setting and displaying the user programmable delays for each of the eight output channels. It also allows the user to monitor optical power levels, VCXO voltage, PC board temperature, optical receiver temperature, and the trigger status of each channel.

The LLNL modified version of the V880.EXE software adds the capability for interfacing with the ITS time measurement instruments. A National Instruments AT-GPIB adapter card is installed in the ITS test PC. The modified software uses the GPIB bus to communicate with the Wavecrest DTS-2075, the RF multiplexer, the digital multimeter. Several GPIB drivers provided by National Instruments provide a means for the V880 PowerBASIC program to talk to each of the GPIB instruments.

A low-level GPIB.COM driver is loaded in the CONFIG.SYS file of ITS test computer. This device driver allows semi low-level programming languages such as C to communicate with the AT-GPIB adapter card. A high-level ULI driver is also installed in the CONFIG.SYS file. This driver enables high-level languages such as PowerBASIC to interface with the GPIB device driver. The ULI driver makes reading and writing to the GPIB bus as easy as talking to standard serial port.

Setting up the Bit3 ISA to VME bus adapter

While setting up the SBS Bit3 Operations Model 403 adapter, several challenges had to be overcome to get the adapter card to work correctly in our test system. Because LLNL is using a similar Bit3 VME to ISA bus adapter as Highland Technology, Highland was able to assist us in overcoming some of our technical difficulties with the adapter. Instructions for setting up the Bit3 adapter card for use in a PC are documented below with the intent that future Bit3 V880 testers will not have to go through the same laborious troubleshooting process.

The following Bit3 settings are known to work with the V880 test software. The AT adapter card can be installed into any ISA slot on a PC, and the VME adapter card must be installed in slot 1 of a VME crate. A cable to connect the two adapter cards is available separately from SBS. The Bit3 adapter card must also be configured to run as the VME system controller, and the default VME address of the V880 adapter should be C000.

The configuration settings used for the Bit3 Model 403 AT adapter are listed below:

CONFIGURATION OPTION	SETTING
PC/AT VMEbus RAM Range	0D0000-0DFFFF (hex)
PC/AT Dual Port RAM Range	Disabled
PC/AT Adapter I/O Range	200-20F (hex)
PC/AT Interrupt Jumpers	None
System Jumpers	None

The configuration settings used for the Bit3 Model 403 VME adapter are listed below:

CONFIGURATION OPTION	SETTING
VMEbus Dual Port RAM Range	Disabled
VMEbus Address Bias	Start At VMEbus Address Zero
VMEbus Adapter I/O Range	C000:DFFF
VMEbus INT Jumpers	None
System Jumpers	VMEbus card drives SYSCLK
Bus Grant and Request Jumpers	Bit3 set as system controller

In addition to these hardware settings, the software configuration files on the ITS Windows 98 workstation also had to be modified. By default, the Bit3 ISA adapter uses

the memory block D000-DFFF. Therefore, the EMM386.EXE line of the CONFIG.SYS file must be written as such: DEVICE=C:\WINDOWS\EMM386.EXE X=D000-DFFF. Care must also be taken to make sure that the BIOS does not cache the memory address occupied by the Bit3 adapter.

How to use the modified V880 test software

After clicking on the icon to start the V880.EXE software executable, a menu of options is presented. To test a V880 DDG, press **D** for “Display Module Data.” Then press “Page Down” until the page 3 is displayed. Page 1 and 2 display the contents of the V880 registers in hexadecimal, while page 3 organizes the information so that it is easier to understand. Page 3 prints the optical power level, the number of good and bad frames, the contents of the V880 status registers, room temperature, PCB temperature, and the optical receiver temperature. Press **O** to turn the V880 trigger channel outputs on. Then proceed to page 4. Page four allows the user to view and modify the control registers for each channel. Press the **A** key to arm all the channels and trigger off the optical data stream.

Pressing page down one more time allows access to the main testing page. From this page, the user can program delays into the V880 DDG, and measure the actual delay using the Wavecrest DTS-2075 time interval counter. The table below outlines the functions available on this page.

Key	What it does
↑	Selects the previous channel on the RF MUX
↓	Selects the next channel on the RF MUX
Time	Changes the delay for the selected channel
Step	Sets the step value
←	Decreases the delay for the selected channel by the step value
→	Increases the delay for the selected channel by the step value
sampRate	Changes the rate at which all output channels are automatically sampled
stepIncr	Changes the time interval between automatic step increases
Begin	Starts an automatic long-term test run, will ask for a file name
End	Ends an automatic long-term test run
On	Enables logging of the monitor channel
ofF	Disables logging of the monitor channel
Help	Activates the on screen help system
<esc>	Exits the Display module Data screen

To set up an automatic long-term test of a V880 module, turn the outputs on and arm all the channels. Then, set the sampling rate of the automatic test by pressing **R** on page 5. The sampling rate is entered in seconds. Make sure that a delay has been set for each of the output channels. After a delay has been set, simply press the **B** key to

begin a test run. Enter a filename to save to; the recommended filename extension is **.CSV**. This makes it easier for Excel to recognize the data file as a comma delimited text file. When it is time to stop the test run, press **E** and the V880 test program will once again be under manual control.

February 22nd, 2000 – SN#101 Test Results

V880 serial number 101 was the first DDG to be tested by the long-term testing software. The SN#101 testing was completed on February 22nd, 2000 using the Noel ITS transmitter. This test proceeded normally with the trigger channel delays set at 900 ns. Channels 0, 2, and 3 closely paralleled each other with measured delays between 70 and 90 ps above 900 ns, while channel 1 was closer to 900 ns with an offset of only 40 to 50 ps. The time-varying delay values were inversely proportional to the PCB temperature, which is consistent with the expected results. The RMS jitter was measured between 4 and 5 ps. However, on this first test run, the V880 test software only recorded one significant digit of jitter, so the jitter graph only shows integer values of 4 or 5.

Although nothing significant was noticed during the 88 hour test of SN#101, a minor problem with the V880 channel control registers was discovered after the test was completed. The control registers incorrectly reported the status of each of the trigger channel outputs. The electrical channels were reported as being optical, and the optical channels were reported as being nonexistent. This problem was documented in NIF-0045108 and is available via PDM. The unit was returned to Highland for repair on March 6, 2000.

March 3rd, 2000 – SN#102 Test Results

V880 serial number 102 completed a 185 hour test run on March 3rd, 2000 using the Noel ITS transmitter. The trigger channel delays were again set to 900 ns. This test proceeded without incident, and time-varying delay values were inversely proportional to the PCB temperature. The RMS jitter values were excellent, with jitters of only 4 to 4.5 ps. The measured delays for all four of the channels were 10 and 50 ps above 900 ns.

April 3rd, 2000 – SN#103 Test Results

V880 serial number 103 completed a 64 hour test on April 3rd, 2000 using the new Facility Timing Transmitter provided by TSC. Three discrepancies were observed and documented. First, the firmware revision of the V880 SN#103 was discovered to be of Revision X, not Revision A (the current officially released version of the V880 firmware). After a discussion with the manufacturer, it was ascertained that Revision X was a working engineering firmware revision, and it should have never been released publicly. Therefore, SN#103 was later sent back to Highland Technology for a firmware upgrade to Revision A (see NIF-0046610)

In addition, a 60 ps jump in measured delay was measured on channel 3 of SN#103. At approximately three hours into the test, the channel jumped from 40 ps above 900 ns to 100 ps. The cause for this jump is yet unexplained.

Lastly, the SN#103 test was performed using a recalibrated Wavecrest DTS-2075 time interval counter. (The DTS-2075 had been returned to Wavecrest after the SN#102 test for a software upgrade and maintenance.) Using the recalibrated instrument, higher RMS jitters of 4 to 8 ps were measured. Measured delays were nominal: between 20 to 60 ps above 900 ns. Similar high jitter measurements were recorded on SN#102 and #104 using the recalibrated DTS-2075. The cause of the higher jitter was later determined to be a result of the DTS-2075 being calibrated at room temperature significantly different from the conditions in Trailer 3907. Since the calibration on the DTS-2075 is only valid for a 5 degree temperature range, the unit was recalibrated at 25 degrees Celsius.

April 10th, 2000 – SN#102 Test Results

The Noel ITS transmitter was used for this 66 hour test run. Jitter was relatively high, measured between 5 and 9 ps. In addition, the delays were measured between 20 and 65 ps above 900 ns. Nothing else unusual was observed.

May 8th, 2000 – SN#104 Test Results

During the May 8th test run of serial number 104 (using the Noel ITS transmitter), several interesting phenomenon were observed. First, RMS jitter was considerably higher than in previous tests (7 to 9 ps). The cause of this was attributed to the Wavecrest not properly calibrated for the room conditions in Trailer 3907. Next, several jumps in measured delays were recorded, and the peak to peak jitter fell to zero in six locations. Upon further analysis, it was discovered that the makeshift ITS transmitter was dropping frames. Over 200 bad frames were recorded during the 113 hour test. Now that the Wavecrest DTS-2075 has been calibrated properly, and the Noel transmitter been adjusted, the SN#104 test will have to be run again.

Summary of problems discovered using long-term V880 testing

- Malfunction of the electrical and optical control register bits in SN#101. For more detail, see the NIF document NIF-0045108.
- The Revision X firmware discrepancy. Two of the four V880 prototypes (103 and 104) had an unofficial release of the V880 firmware installed. These units have since been upgraded to the official Revision A.
- The unexplained jump in measured delays for channel 3 on SN#103 during the April 3rd test.
- Serial number 104 was discovered to have lost its calibration table after having been used extensively in the PAM module. The battery backed RAM may have been affected by a static discharge. See NIF-0046610

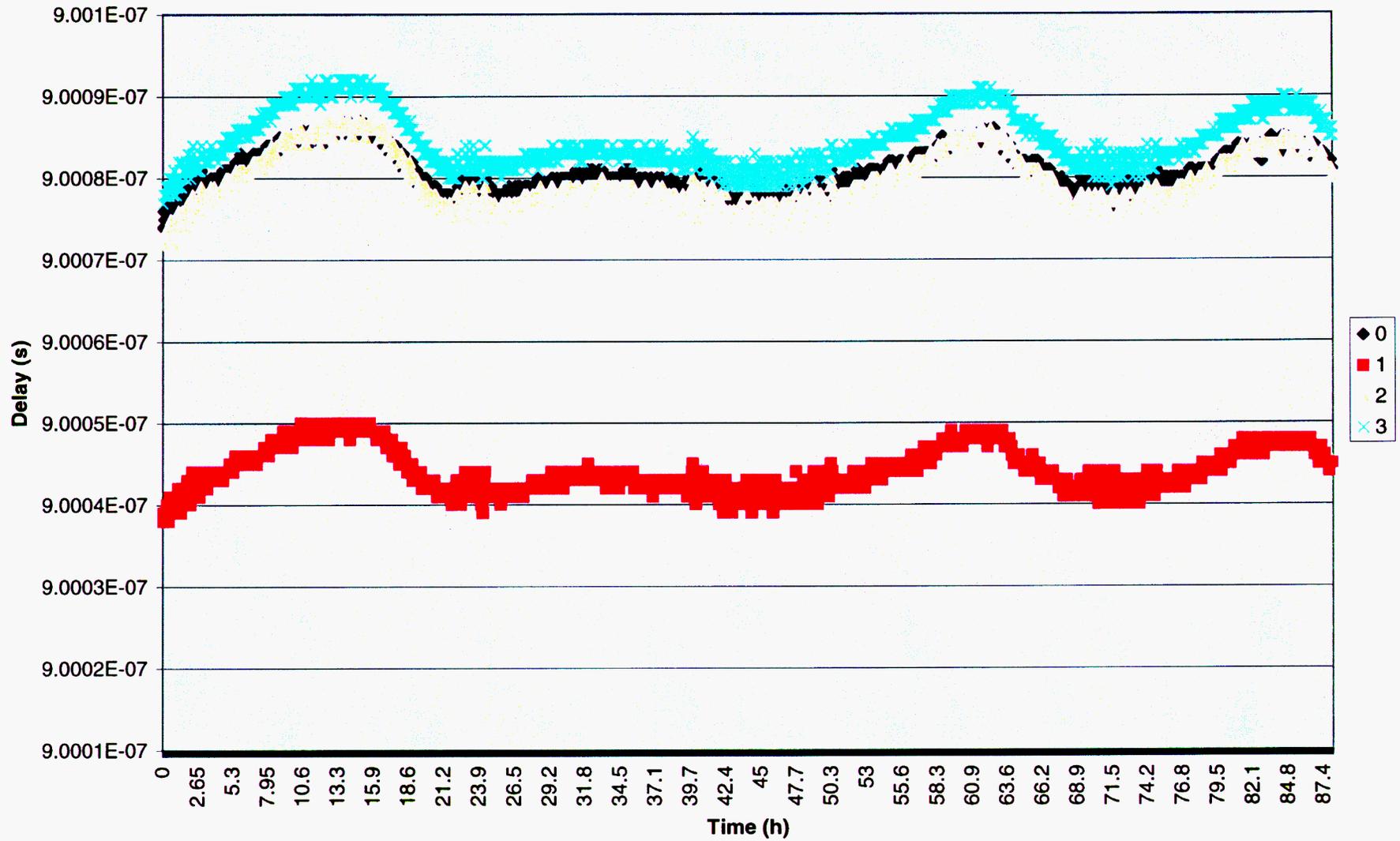
- High jitters during the May 8th SN#104 test prompted the ITS test team to perform a internal calibration on the Wavecrest DTS-2075 to compensate for the room temperature in Trailer 3907.

Comments

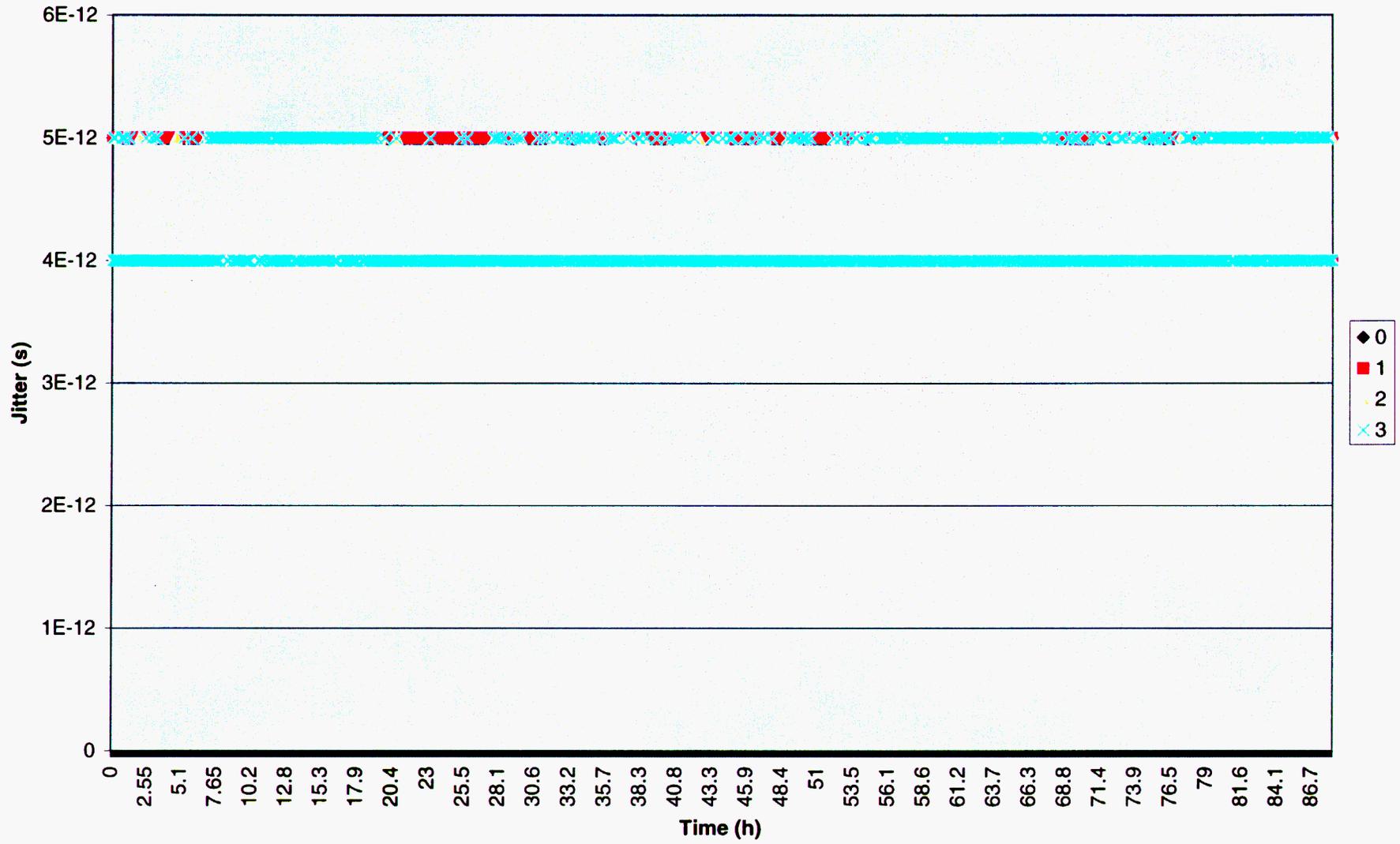
Continued long-term testing of the V880 delay generators will be needed to determine possible drift characteristics and variations caused by temperature variations. Each of the tests performed thus far have compared the trigger channel output against the compensated reference channel on the V880. While each output channel compensates for the drift associated with temperature changes, the reference channel does not. This accounts for the inverse relationship observed between the temperature and fluctuations in the measured trigger channel output delays. The Revision B V880 modules are expected to arrive in August 2000, and these will include temperature compensated reference channels. The long-term V880 tests will need to be repeated with the new Revision B modules. However, in order to appropriately test the V880 trigger channel outputs, it will be necessary to compare the outputs against an external frame sync rather than the V880 reference channel. This improvement is currently being worked on.

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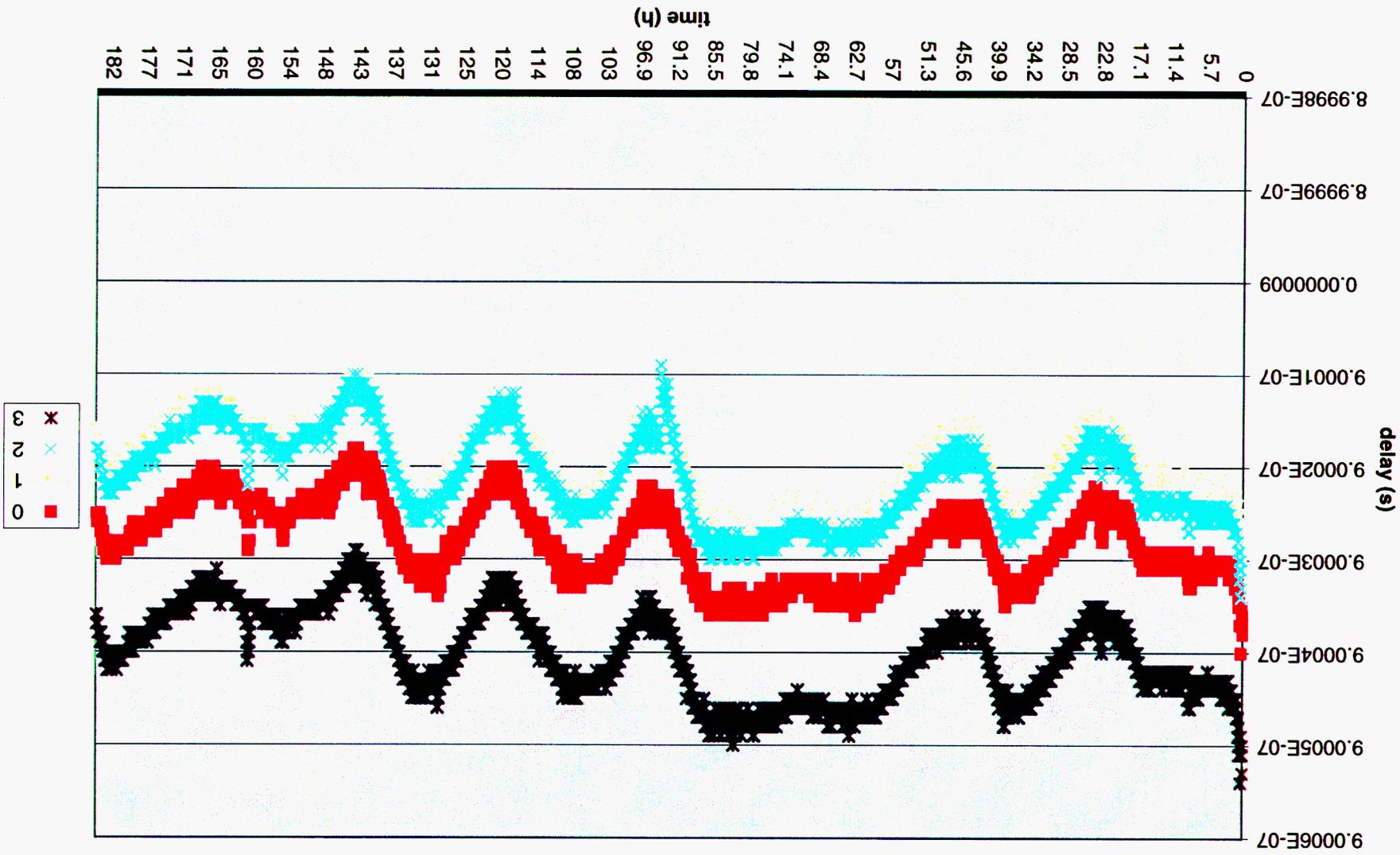
Time vs. Measured Delay for SN#101 (February 22nd, 2000)



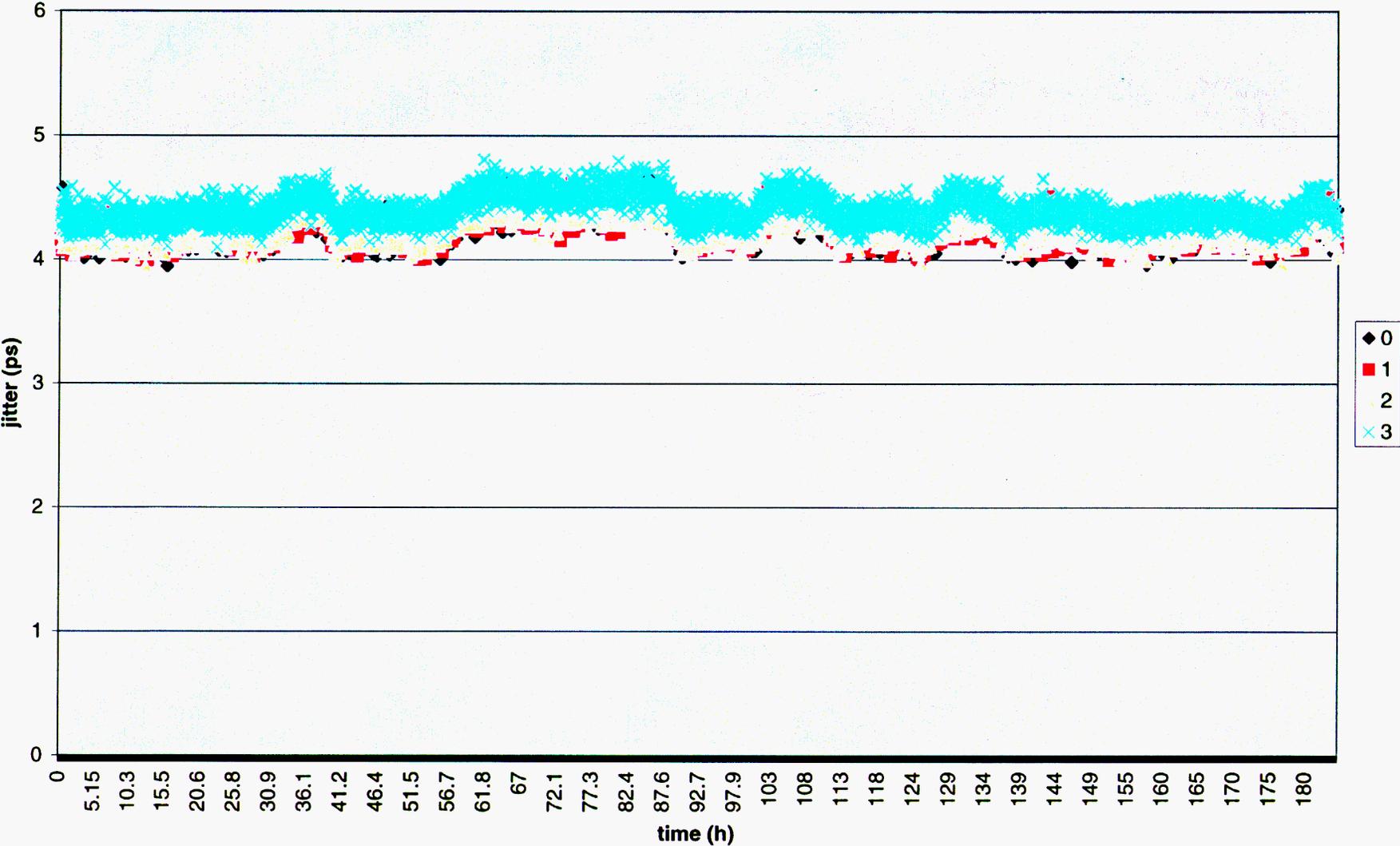
Time vs. Jitter for SN#101 (February 22nd, 2000)



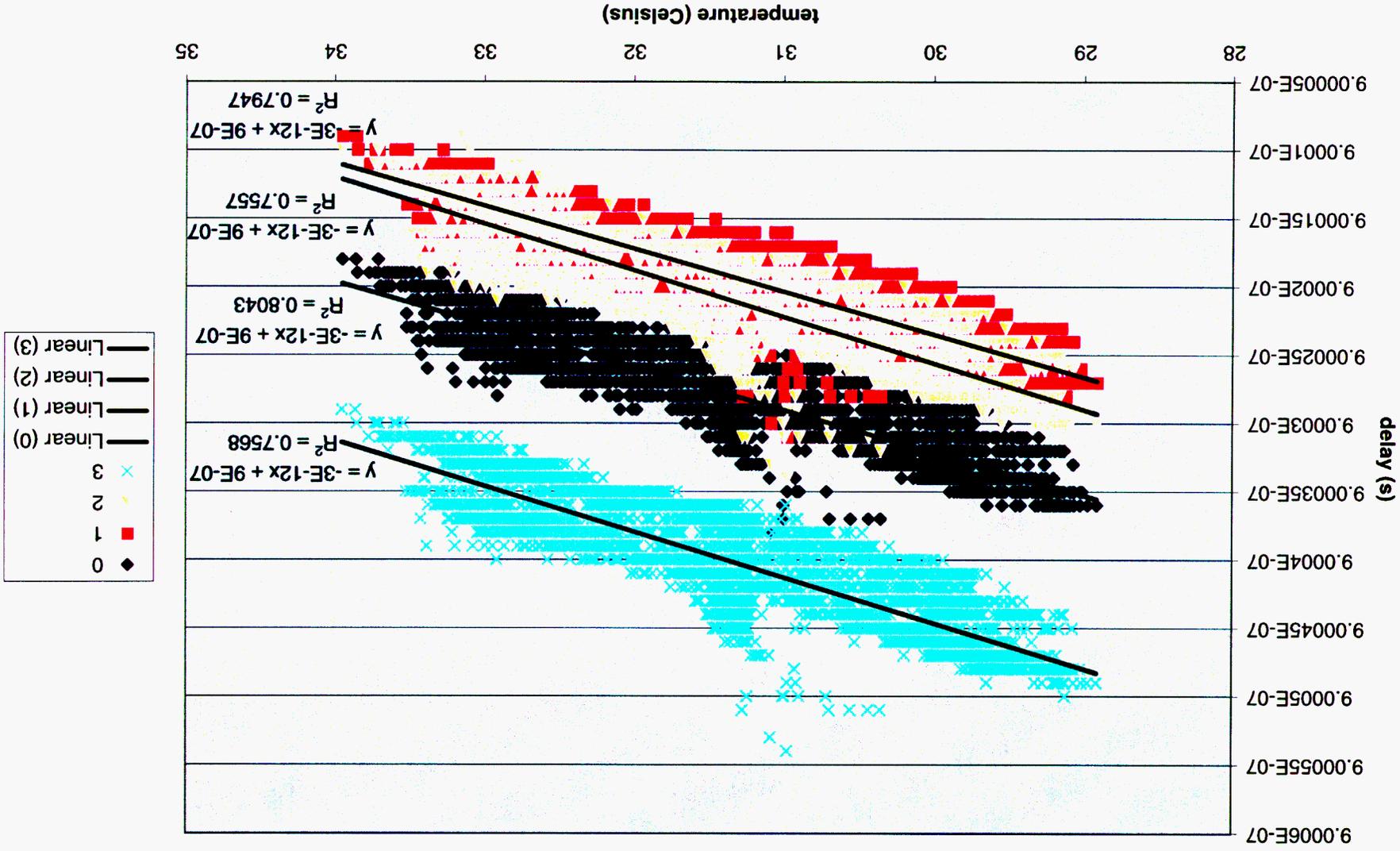
Time vs. Measured Delay for SN #102 (March 3rd, 2000)



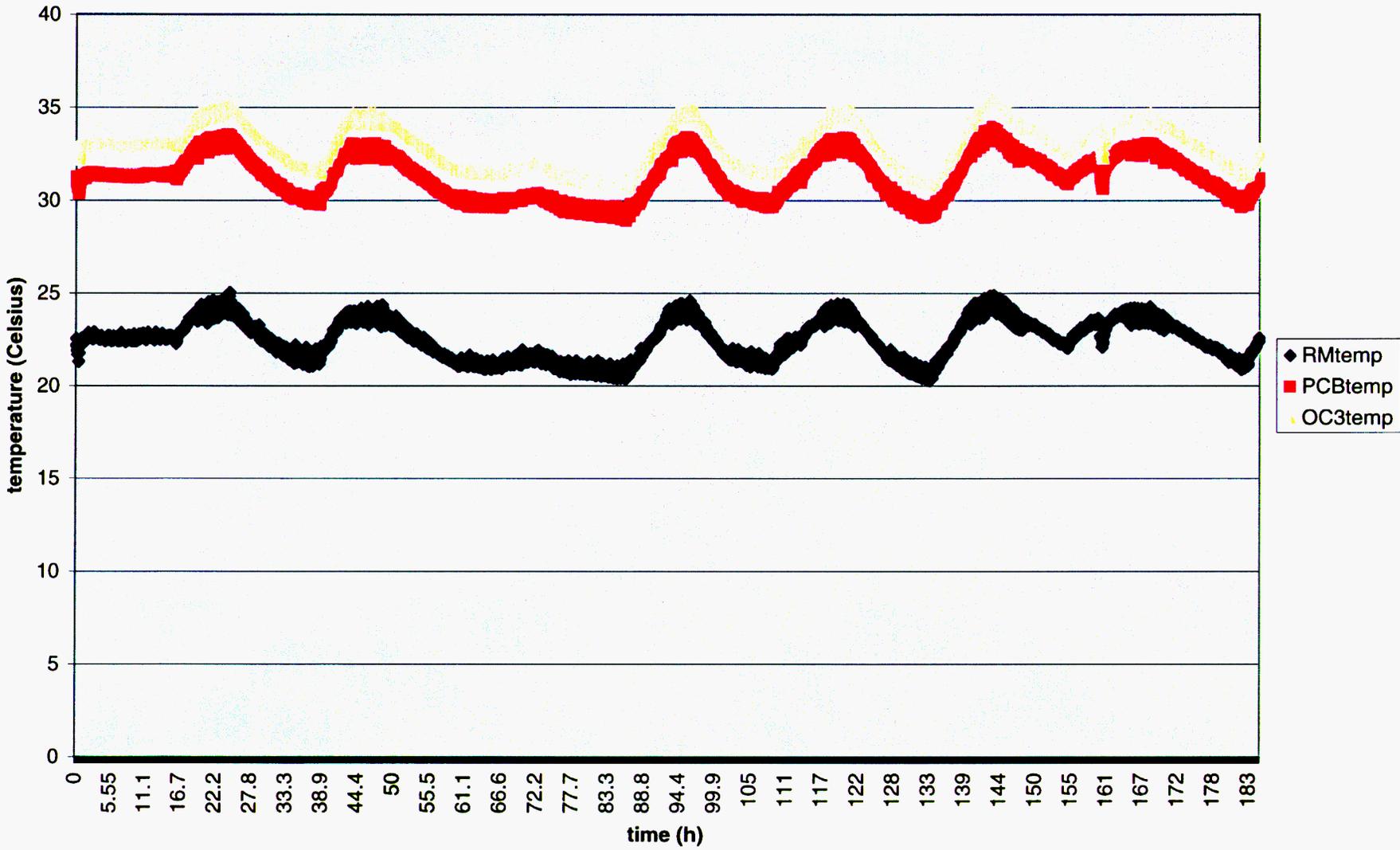
Time vs. Jitter for SN #102 (March 3rd 2000)



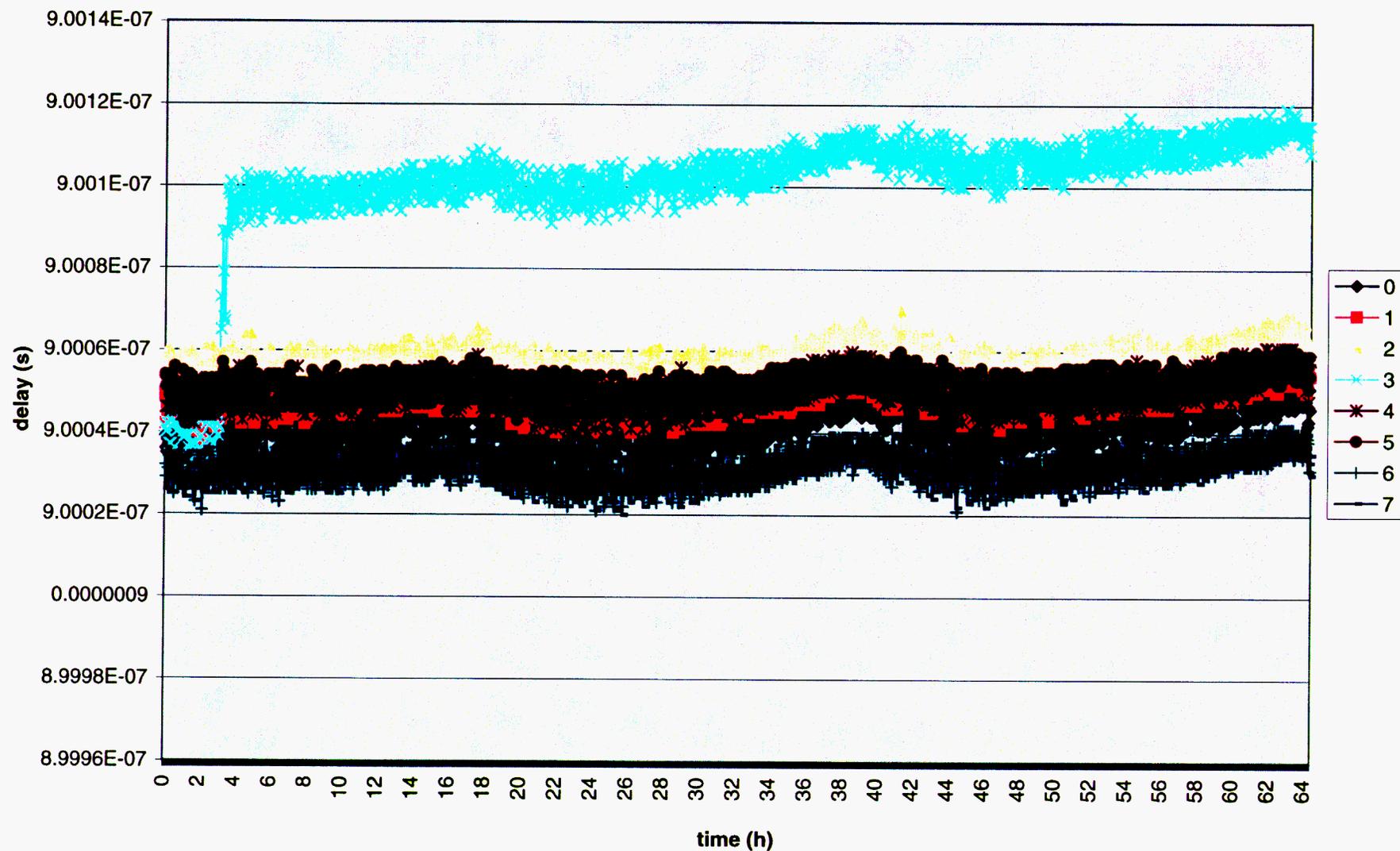
Temperature vs. Delay for SN #102 (March 3rd, 2000)



Time vs. Temperature for SN #102 (March 3rd, 2000)



Time vs. Delay for #103 (April 3rd 2000)



Time vs. Temperature for #103 (April 3rd 2000)

