THRUST AREA REPORT • UCRL-ID-129203

Microtechnology

Raymond P. Mariella, Jr.,
Thrust Area Leader

This is an informal report intended primarily for internal or limited external distribution. The opinions and conclusions stated are those of the author and may or may not be those of the Laboratory.

Work performed under the auspices of the U.S. Department of Energy by Lawrence Livermore National Laboratory under Contract W-7405-Eng-48.

January 1998

Disclaimer

This document was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor the University of California nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial products, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or the University of California. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or the University of California, and shall not be used for advertising or product endorsement purposes.

This report has been reproduced
directly from the best available copy.

Available to DOE and DOE contractors from the
Office of Scientific and Technical Information
P.O. Box 62, Oak Ridge, TN 37831
Prices available from (615) 576-8401, FTS 626-8401

Available to the public from the
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Rd.,
Springfield, VA 22161

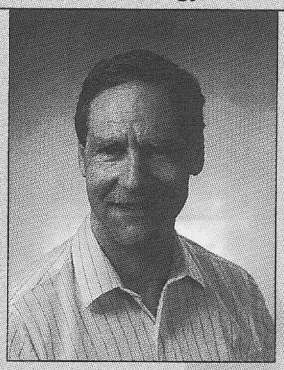
THRUST AREA REPORT • UCRL-ID-129203

Microtechnology

Raymond P. Mariella, Jr.,
Thrust Area Leader

Reprinted from Engineering Research, Development and Technology
FY 97 UCRL 53868-97

January 1998



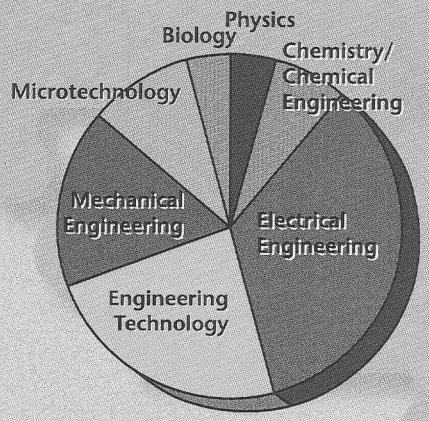
Raymond P. Mariella, Jr., Thrust Area Leader

The Microtechnology thrust area conducts activities for the Lawrence Livermore National Laboratory (LLNL) missions of global security, global ecology, and bioscience. Our efforts are associated with devices, instruments, or systems that require microfabricated components, including micro-electromechanical systems (MEMS), electronics, photonics, microstructures, and microactuators.

All of our microtechnology work revolves around our microfabrication facility. In all work, we have close collaborations with the various LLNL programs, ensuring that we select those areas for our attention that offer the greatest leverage to LLNL.

Our work is driven principally by the applications of our internal programs, and, to a lesser extent, by external applications. For both of these we must have interdisciplinary teams to deliver complete solutions to the problems. Our recent successes in analytical instrumentation reflect our broad, interdisciplinary base and the cross-fertilization that results from all of the personnel sharing their capabilities and ideas with each other.

The Center for Microtechnology continued to grow in FY-97. The more than 60 people working in this thrust area have training as shown in the following figure:



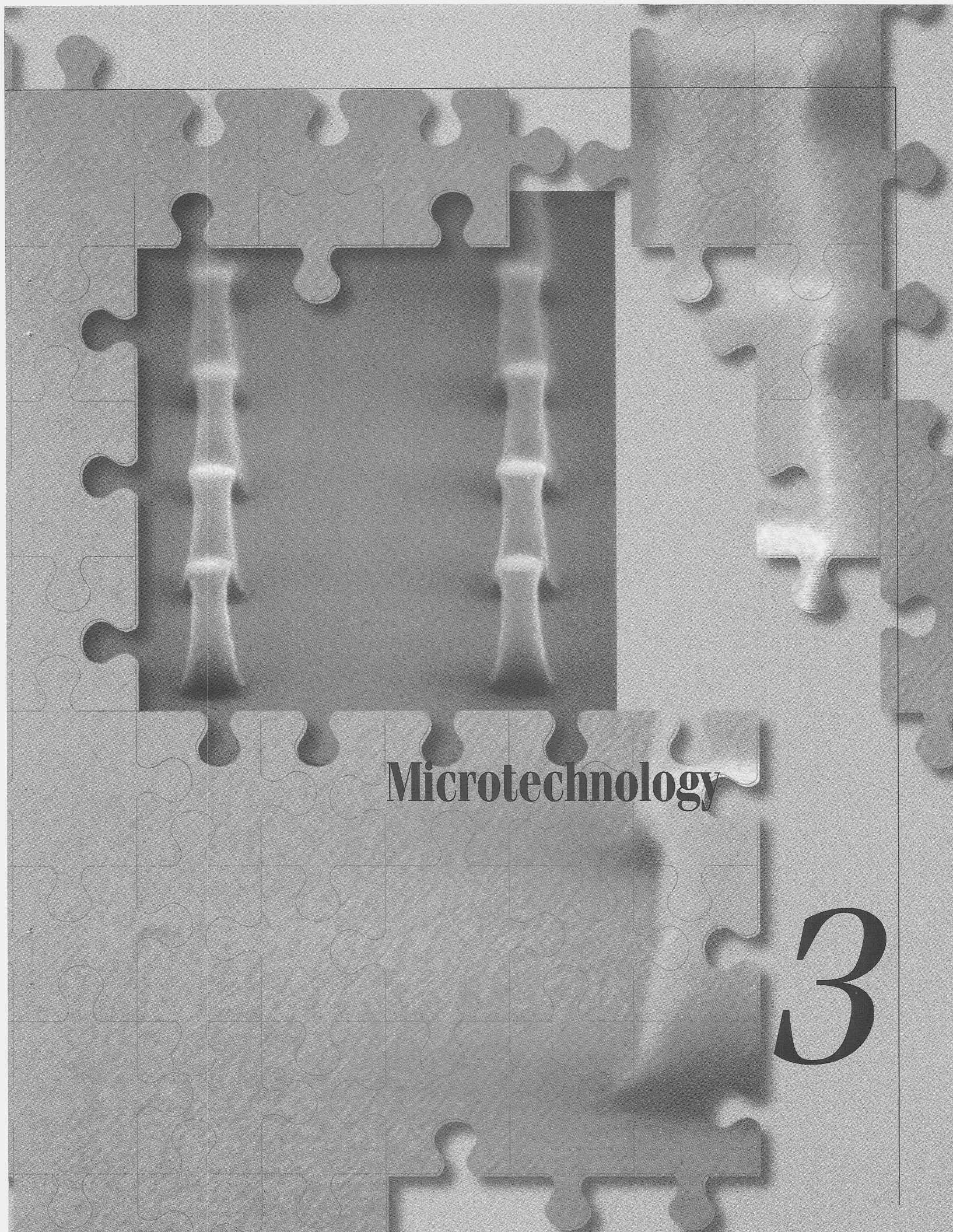
We continue to show a very high rate of return on investment. Over the last year, with a total budget of over $13M, including approximately $0.5M of technology-base projects, we have successfully performed collaborations with industry. We have had one instrumentation project for performing automated, multi-chamber, real-time polymerase chain reaction for DNA amplification funded by the Defense Intelligence Agency. One microtechnology project in collaboration with University of California, Santa Barbara (UCSB) researchers successfully produced the first GaN laser in the United States.

In the fall of 1996, we took our flow cytometer (invented under Engineering TechBase funds) to the Joint Field Trials (JFT) in Dugway, UT, for the open competition and scored the best performance ever recorded there for detection of the Anthrax simulant (Bacillus globigii).

Overall, numerous small technology-base investments in microtechnology have paid off this year:

1) outstanding results at JFT III with the LLNL flow cytometer, miniFlo;
2) highest performance hand-held gas chromatograph built;
3) automated PCR system at Dugway PG for the Navy port/airbase ACTD;
4) LLNL electrophoresis system with etched/bonded plates—a future keystone in the Department of Energy's Joint Genome Institute/Human Genome Project in LLNL's Biology and Biotechnology Research Program;
5) $1M DARPA funding for dielectrophoresis technology;
6) $1M CRADA signed using shape-memory-polymer release mechanism in medical applications;
7) $2.2M external funding for optical interconnects in partnership with the Photonics Program;
8) highly visible multi-$M CRADA with Intel Corporation and other semiconductor houses for EUV lithography (the Microtechnology Center is being expanded to accommodate this work); and
9) collaboration with UCSB and the country's first GaN laser.

As the applications for microtechnology grow, we continue to perform the technology-base activities for LLNL and external partners and stay in a leadership position, both nationally and world-wide.



Microtechnology

3

3. Microtechnology

Overview
Raymond P. Mariella, Jr., Thrust Area Leader

Gas and Vapor Preconcentrator
Conrad N. Yu, Jackson C. Koo, and Norman F. Raley 3-1

Compliant Silicon Nitride Cantilever Beams for Atomic Force Microscope Applications
Dino R. Ciarlo 3-3

Sub-Micron Lithography
Dino R. Ciarlo 3-5

Complementary Metal-Oxide Semiconductor Electronics and Micro-Electro-Mechanical Systems
Charles F. McConaghy and Abraham P. Lee 3-7

Monolithic High-Performance Three-Dimensional Coil Inductors for Wireless Communication Applications
Vincent Malba, Darrin J. Young, Jia-Jiunn Ou, Anthony F. Bernhardt, and Bernhard E. Boser 3-11

Vertical-Lasing Semiconductor Optical Amplifiers
Jeffrey D. Walker and Sol P. Dijaili 3-17

Field-Emission Cathode Micro-Electro-Mechanical System Technology for Sensors, Diagnostics, and Microelectronics
Jeffrey D. Morse, Jackson C. Koo, Robert T. Graff, Alan F. Jankowski, and Jeffrey P. Hayes 3-21

Blue Laser Diode Process Development
Glenn A. Meyer, Gregory A. Cooper, Stacy L. Lehew, and Steven DenBaars 3-25

Laser Transceiver for Safeing Applications
Charles F. McConaghy and Karla G. Hagans 3-31

Gas and Vapor Preconcentrator

Conrad N. Yu, Jackson C. Koo, and Norman F. Raley
Engineering Research Division
Electronics Engineering

We have investigated multiple-fine-hole and slot-structures on silicon wafers as gas and vapor preconcentrators for the portable gas chromatograph (GC) application. Our calculation and test results indicated that the surface areas of these structures are too small to be useful. We plan to redesign these devices for the portable GC application.

Introduction

A gas and vapor preconcentrator is commonly used in ordinary GCs to increase their detection capability and sensitivity. For this case, we have to make the preconcentrator not only miniature, but also compatible with the fabrication technique of the portable GC. In short, we need to produce these preconcentrators by micro-electro-mechanical systems (MEMS) technology.

Progress

From our early experiments, we measured several parameters of the portable GC: the gas flow velocity, V, was about 5 cm/s; the sample signal duration, T, about 10 ms; and the diameter, D, of the separation column, 100 µm. From these numbers, we calculate the gas sample size, v, required for the portable GC ($v = \pi VT(D/2)^2$) to be 4 nL. The injection duration in the portable GC is required to be the same as the sample signal duration, 10 ms.

For a sample preconcentrator, sample gas will first have to be adsorbed on its surface. A material with a large surface area is required. Nano-porous silicon has a high specific surface area, about 100 to 600 m^2/cm^3, but is somewhat limited in robustness. We chose to first investigate silicon membrane structures in several different sizes, with multiple fine holes and slots. The specific surface areas of these devices is quite a bit lower, with values ranging from 0.2 to 0.3 m^2/cm^3.

The primary structure first investigated is shown in **Fig. 1**. The total size of the membrane of the devices is 1 mm × 1 mm × 50 µm. The total surfaces, S, are calculated to be from 10 to 15 mm^2. To calculate or estimate the amount of adsorbed monolayer of gas sample, we used water as an example. The diameter of a water molecule is 2.5 Å; the total adsorbed water volume, v(w), is 37.5×10^{-10} cm^3. Since the surface water density, d, is 1 g/cm^3, there are $n = v(w)d/18 = 0.21$ nmoles of water. At high temperature, under standard pressure, the steam volume becomes 4.67 nL.

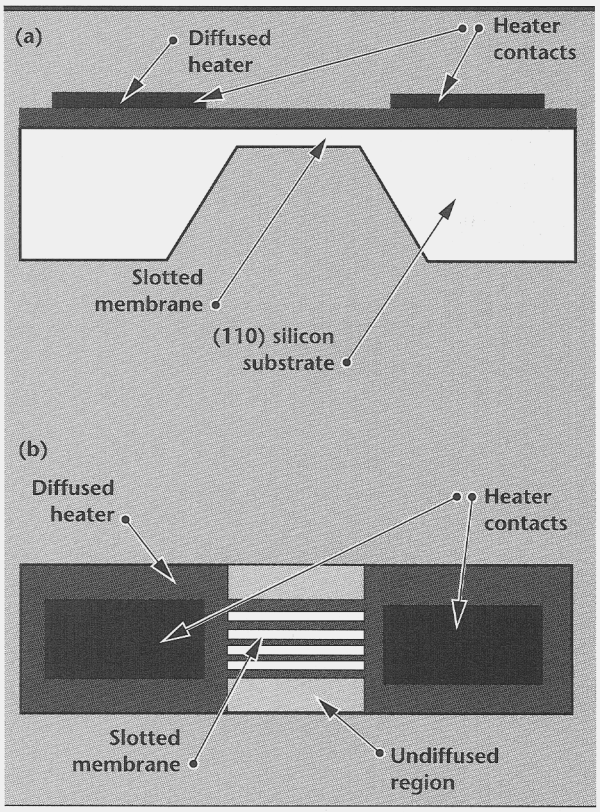


Figure 1. Schematic illustration of two silicon membrane structures: (a) with holes, and (b) slotted.

The top surfaces of these silicon membranes are phosphorous-doped to achieve a diffused heater with a surface resistance of 18.6 Ω per square. Two metal electrodes are placed on each side of the same top surfaces of the membranes. Resistances of these devices are measured, with values typically more than 70 Ω. To evaporate the amount of adsorbed material within 10 ms, we have to increase the device temperature within this duration above the evaporation temperature, in general, around 100 °C.

To ensure the localization of the heating, we fabricated these devices again by placing the electrodes on the opposite sides of the silicon membranes. Their resistances were measured to be somewhat less than 50 Ω. The weight of the silicon membrane is calculated to be 110 µg; its heat capacity is 0.7 J/g K. Because of the small amount of adsorbed sample molecules, and because of the good insulation characteristics of air without convection, heat loss due to adsorbed molecules and the surrounding air can certainly be neglected. Due to the small cross-sectional area and the short duration, we also neglect the heat conducting out of the membrane region in our calculation of heating power. The heating power required can then be shown to be 0.8 W.

To ensure rapid temperature rise, we applied a 12-V power supply directly onto these devices. The heating power was about 4 W. The temperature of the device increased quite rapidly. Direct temperature measurement, however, is quite difficult, due to the small membrane size. For the adsorbed gas samples, we expected to observe the evaporating steam from its surface, the effect of expansion of the heated gas in a small volume, or some acoustic effect.

However, in our tests, no visible emission of gas, steam, or acoustic effect was observed, with or without small paper cover. The amount of gas or steam generated seemed to be much smaller than what is calculated.

In practice, because the sample concentrator needs to be in a certain size enclosure, and because the sample gas produced needs to have higher pressure than that in the separation column, to inject the sample gas into the separation column in 10 ms, the volume required in a portable GC should be one or two orders of magnitude more than what is calculated. In other words, the steam volume due to the monolayer-adsorbed water molecules is too small for the portable GC application.

In summary, we have designed and fabricated silicon membrane structures with various holes and slots. Our calculation and test results showed that the gas volumes generated from monolayer adsorption are too small to be useful. We have to redesign these devices for the GC application.

Future Work

From the above experimental results, we think the basic approach of the preconcentrator is sound, but the total available surface area may need to be adjusted. We also need to consider and develop the preconcentrator concurrently with an injector or a sniffer. They may have to be considered and designed together as a unit. There may also be other materials and coatings to be considered in future fabrication.

Compliant Silicon Nitride Cantilever Beams for Atomic Force Microscope Applications

Dino R. Ciarlo
Engineering Research Division
Electronics Engineering

Silicon nitride cantilever beams were fabricated for use in Atomic Force Microscopes. Depending on their design, these beams can be more compliant than those commercially available. This gives experimenters another source for these cantilever beams when the force exerted on their sample needs to be kept to an absolute minimum.

Introduction

There is a proliferation of Atomic Force Microscopes (AFMs) at Lawrence Livermore National Laboratory (LLNL). These instruments analyze surfaces or material on surfaces by dragging a sharp stylus across the surface and monitoring the position of this stylus. The monitoring is done optically or with a piezo-resistive sensor.

The instruments can achieve Angstrom-level vertical resolution, and are used extensively in microfabrication, by biologists and by most surface scientists.

Normally, the manufacturer of the AFM offers a variety of styluses, depending on the application. They are usually small cantilever beams made of silicon or silicon nitride, with sharp points on one end. Occasionally an experimenter requires a stylus with a compliance (flexibility) not available from the manufacturer. This proposal describes styluses fabricated from our low-stress silicon nitride process.

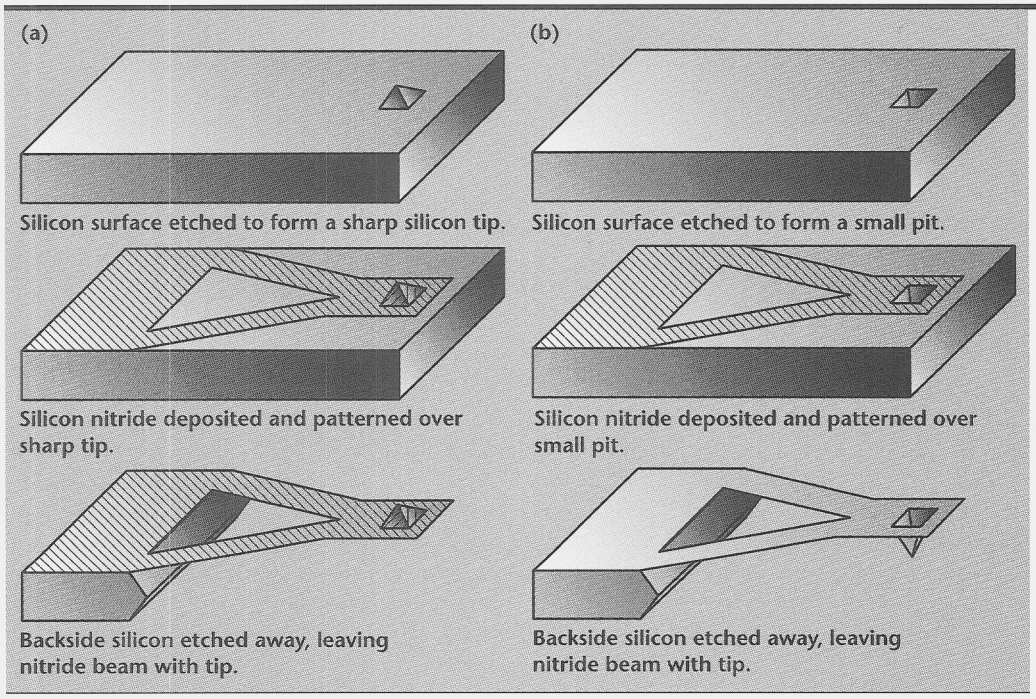


Figure 1. Fabrication sequence for two types of silicon nitride cantilever beams for AFM applications.

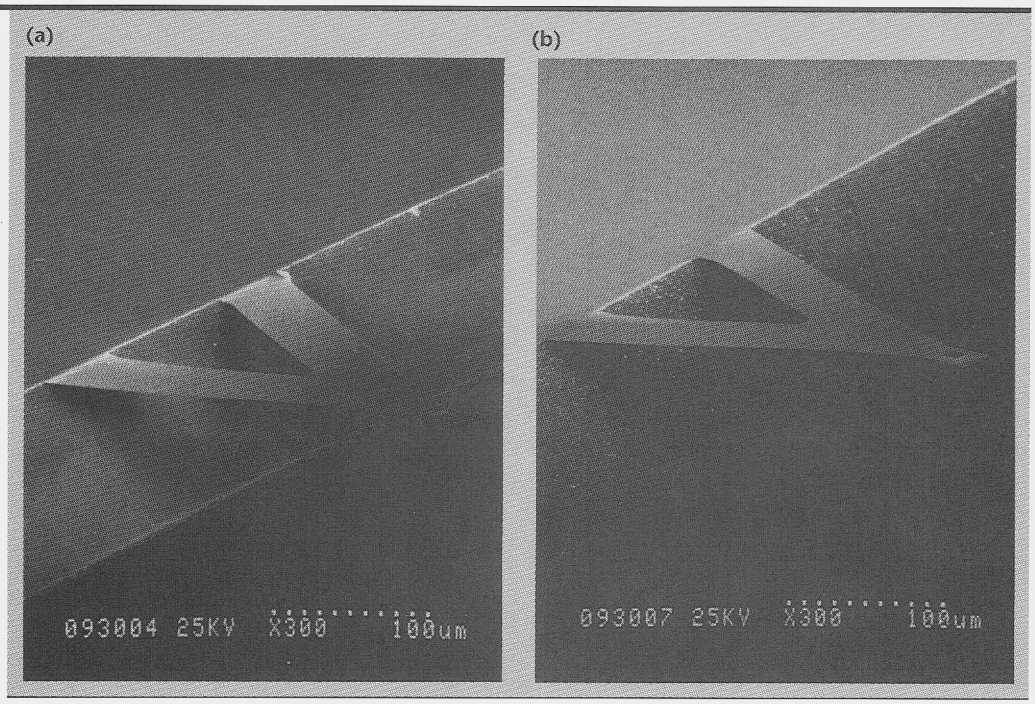


Figure 2. SEMs of silicon nitride cantilever beams, 500 nm thick and 200 µm long. The sharp point on the end of the cantilever extends upward in (a) and downward in (b).

Progress

We fabricated compliant silicon nitride cantilever beams of two designs, as illustrated in **Fig. 1**. Both used 200-µm-thick silicon wafers, with double-sided polished (100) surface orientation, and 50-mm diameter. In the first design, a small, four-sided pyramid was first etched through a small silicon nitride square mask into the surface of the wafer, using an anisotropic wet etch (potassium hydroxide). This pyramid was then covered with a 500-nm-thick film of our low-stress (300 MPa) silicon nitride. The silicon was then etched away from the back of the wafer to release the suspended cantilever beam, 500 nm thick.

In the second design, a sharp silicon point was first formed by etching the silicon surface that had been covered with a small silicon nitride mask. We used an isotropic etch (hydrofluoric-nitric-acetic). This point was then coated with the same low-stress silicon nitride. As before, the silicon was then etched away from the back of the wafer to release the 500-nm-thick cantilever beam.

Figure 2 shows SEMs of the results. Each cantilever is supported by a silicon holder with overall dimensions of 3.5 mm × 1.5 mm. This is close to the part size used by several AFM vendors. On each 50-mm-diameter silicon wafer, we fabricated 90 separate devices, changing the shape of the cantilever in groups of five. The shortest cantilever is 100 µm long, while the longest is 500 µm.

Apparently there is no stress gradient through the thickness of our nitride, because the cantilevers are very straight and flat. Some care had to be taken during the rinse after the etch to prevent the cantilever beams from collapsing from capillary action. Of the two types of cantilevers fabricated, the one shown in **Fig. 2a** is more practical, since the silicon holder does not limit the size of the sample to be measured. For the cantilever shown in **Fig. 2b**, the sample size needs to be comparable to the length of the cantilever beam. There are ways to eliminate this limitation by using wafer-to-wafer silicon bonding.

Future Work

These new cantilever beams should be tested in a real instrument. Since a wide variety of beam lengths and shapes were fabricated, it is likely that an optimum design can be selected. If not, these tests would supply enough information to optimize the design during the next fabrication run.

Sub-Micron Lithography

Dino R. Ciarlo
Engineering Research Division
Electronics Engineering

We continued to investigate the use of phase shift masks to improve the lithography performance of a commercial wafer stepper. Our effort this past year concentrated on the use of double exposure schemes to print small diameter columns in photo-resist, on anti-reflection coatings, and on the installation of the lithography simulation program known as Sample3D from the University of California, Berkeley (UCB).

Introduction

In previous work, we reported on the improvement of the lithography capability of a 1X Ultratech wafer stepper by the use of phase shift masks.[1] Line-widths were printed in positive photo-resist that were 0.2 µm wide, using a system with a specified minimum resolution of 0.7 µm.

Phase-shift masks adjust the phase of the UV radiation going through the mask to take advantage of interference effects. In the type used in this work, the phase of the electric field is shifted by 180° for adjacent sections as the radiation exits the mask. The exposure energy arriving at the wafer plane is proportional to the square of the magnitude of the electric field. Therefore, this exposure energy is positive on both sides of the phase-shift edge, but it has a true zero value at the edge. This leads to a very narrow line of unexposed resist.[1] As in the past, all our experiments were performed at Ultratech Stepper, in San Jose, California, using their SATURN 1X stepper.

Progress

During this past year, we experimented with double exposure schemes to print small diameter posts. The advantage of this scheme is that it allows one to print small diameter posts without having to have small features on the mask. For example, we used a phase-shift mask consisting of parallel lines that were 2 µm wide. The phase-shifts of these lines alternated between 0° and 180°.

If this mask is first printed in one direction at a reduced intensity, and then printed again after being rotated by 90°, the result is an array of small diameter columns located at the intersection of the edges in the two exposures.

An SEM of such an experiment is shown in **Fig. 1**, demonstrating that an array of sub-micron diameter posts can be printed from a mask consisting only of 2-µm-wide lines.

A critical parameter in these experiment is the exposure intensity required. For our experiments we use the JSR 500 positive resist, with a nominal

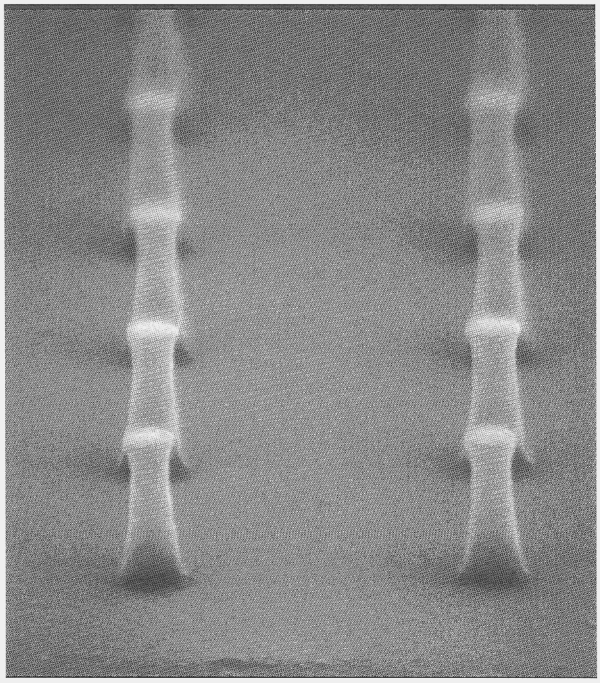


Figure 1. Photo-resist posts, 0.3 µm in diameter, printed using the double exposure of a phase-shift mask. Center-to-center spacing is 2 µm.

thickness of 1 µm. The minimum i-line (365 nm) UV energy required to clear this resist is 100 mJ/cm^2. The two exposures used in **Fig. 1** were both 75 mJ/cm^2.

We also experimented with anti-reflection coatings (ARC). Most of our initial results were obtained on bare silicon wafers coated with photo-resist. A more practical application is to print resist images on a silicon wafer that has been coated with a metal. We used a 60-nm coating of cobalt for our experiments, and found that the smallest feature that could be printed using phase-shift masks, was about 0.8 µm, as compared to 0.2 µm, printed on bare wafers.

This is most likely caused by the change in reflectivity of the cobalt, as compared to the bare silicon. A couple of experiments were tried with a commercial ARC, having a thickness of 200 nm. The results were not very different, meaning that the thickness of the ARC layer, or perhaps the type of ARC layer needs to be changed.

Finally, we successfully installed the UCB lithography simulation program, called Sample3D, on our UNIX work station to help guide and understand our lithography experiments. This is a powerful simulator that allows one to simulate the resist profiles resulting from various exposure tools and different resists. Input to the program consists of the mask design, a description of the exposure tool and the photo-resist parameters. The output is an aerial image of the exposure energy at the wafer plane and a three-dimensional image of the developed photo-resist pattern.

Future Work

Through the combined efforts of The Advanced Microtechnology Program (AMP) in Lawrence Livermore National Laboratory's Laser Directorate and Electronic Engineering Technology Division, a 5X wafer stepper has been purchased, and will be installed in the MicroTechnology Center early in FY-98. Our plans are to apply the advanced lithography techniques we have developed to this new tool.

References

1. Ciarlo, D. R., and D. R. Kania (1996), "Phase-Shift Lithography," *Engineering Research, Development and Technology FY96 Thrust Area Report,* Lawrence Livermore National Laboratory, Livermore, CA, (UCRL 53868-96).

Complementary Metal-Oxide Semiconductor Electronics and Micro-Electro-Mechanical Systems

Charles F. McConaghy and Abraham P. Lee
Engineering Research Division
Electronics Engineering

The goal of this technology-base project at Lawrence Livermore National Laboratory (LLNL) has been to build the infrastructure in electronics support for our micro-electro-mechanical systems (MEMS) activity in the Microtechnology Center. Included in our goal is the ability to fabricate electronics at the chip level, and meld this with the MEMS device. A secondary purpose of this project has been to develop capacitive positioning electronics for use with a MEMS moveable mirror.

Introduction

We generally require electronics to use MEMS devices in real applications. Devices such as the gas chromatograph, the miniature polymerase chain reaction (PCR), or moveable mirrors, all require electronics before they can be put into a functional system. The electronics can be completely external to the MEMS device, but it is desirable to have some functions integrated, or co-located, to reduce parasitic capacitance as well as physical size. Further advantages might be in power saving, ease of fabrication, and more functionality to the end user.

Two Approaches to Integration

One method of incorporating electronics is to have a completely integrated process, an approach used by Analog Devices and Sandia National Laboratories. The completely integrated process has both complementary metal-oxide semiconductor (CMOS) electronics and MEMS devices fabricated on the same chip. Therefore, both electronic processing for devices such as amplifiers and switches, and mechanical processing for devices such as proof masses and comb drives, take place in the fabrication procedure. Because the electronic and mechanical devices reside on the same physical piece of silicon, these processes must be carefully tailored to meet the constraints of both types of devices. Often trade-offs must be made, in the type of electronic or mechanical devices that can be fabricated.

A second approach is to fabricate the electronics and MEMS devices separately, and to bond them together afterwards. The advantage of this approach is that the processing can be optimized for each type of device. For example, sub-µm CMOS can be easily combined with deep-etched MEMS structures. The disadvantage is that the devices then need to be bonded together. Parasitic capacitance might also be slightly higher, because longer interconnects may be needed to mate the two types of devices. However, because of the flexibility and the ability to use outside resources such as the Berkeley Sensor and Actuator Center (BSAC, Berkeley, California), MOSIS (University of Southern California), and the MEMS Technology Application Center (MCNC, North Carolina), this is the approach we have taken to meet our objectives.

Progress

The Micro-Mirror Project

A related project, to fabricate a miniature moveable mirror by MEMS, was chosen as the demonstration MEMS project that would use the CMOS electronics. The MEMS mirror, a 1-mm square piece of polysilicon that moves 1200 nm, in and out of the plane of the silicon substrate, was designed as a replacement for large piezo-driven phase-shifting mirrors. The voltage levels to drive this mirror are less than 10 V. However, the mirror movement is slightly non-linear. When used in one arm of an interferometer, the movement of the mirror causes phase-shifting of the light, which translates to movement of fringes in the interferometer. It is desirable to have the movement of the mirror and the resulting fringes as linear as possible.

Capacitive position sensing

Capacitance is used in many MEMS devices, such as accelerometers and pressure sensors, to determine position or amount of movement. Typically, one plate of the capacitance sensor is formed by the moveable structure, with the other plate formed by the substrate or some fixed structure, such as the anchored part of a comb drive. Therefore, as the moveable part changes position, the capacitance varies inversely with displacement. This assumes a parallel plate approximation for the capacitance, which is a reasonable assumption in the case of our micro-mirror. Actual capacitance values range from femptofarads to a few picofarads.

One of the challenges in capacitive sensing is to separate the sense capacitor signal from the often larger parasitic capacitances of the MEMS structure. For example, the mirror sense capacitance is about 2 pf, whereas the capacitance of the bottom sense plate to the substrate is on the order of 50 pf. Clever circuit topologies that involve keeping the voltage across the parasitic capacitances near zero, minimize the impact of the parasitics.

One circuit that we tried initially used a switched current approach, where a current source was applied to the sense capacitor for a known time, depositing a known amount of charge, which resulted in a voltage proportional to the sense capacitor value. Although this technique worked, it required that voltages on the order of a few volts be present on the capacitor. Voltages greater than 1 V on our large-area sense capacitor caused an electrostatic force which was directly opposite to the force of the comb driver force, and tended to interfere with the movement of the mirror.

A second capacitive-sensing technique, shown in **Fig. 1**, uses a very low-amplitude high-frequency signal (well above the mechanical frequency of the mirror) to sense the change in the capacitance impedance as the position changes. The detector uses synchronous detection to filter out all but the probe signal.

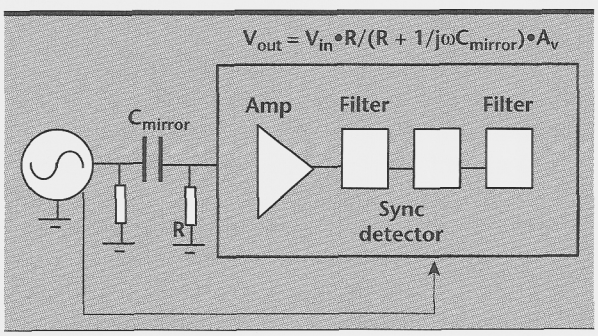


Figure 1. Capacitive sensing circuit using a low-amplitude high-frequency probe signal.

The circuit of **Fig. 1** was first implemented on a 1-in.-×-1-in. surface mount board that contained all the electronics and the MEMS mirror. The electronics system was useful as a diagnostic of the mirror movement. The circuit showed that the mirror had response times of 20 ms and 200 ms for upward and downward movement, respectively. In addition, the sense circuit showed the linearity of mirror movement as a function of drive voltage.

One additional piece of information that the circuit yielded was the starting position of the mirror. The calculated values of capacitance, based on a simple model for two parallel plates separated by 2 µm, did not agree with the measured starting capacitance. This led to optical measurements of the mirror with a Zygo interferometer, which showed that the mirror plate was somewhat bowed from stresses induced by the supporting MEMS springs.

The conclusion was that the amount of bowing was not completely predictable, thus making absolute distance measurements with the capacitance sensor not easily obtainable. However, even with the bow, the mirror movement still follows the inverse relationship with capacitance, thus making the relative position obtainable. Therefore, the capacitance can be used for linearization of movement, since the absolute position is not necessary for this application.

Figure 2 shows the capacitance signal as the micro-mirror is driven over a distance of 1200 nm. In one case the mirror is driven by a linearization look-up table; in the other, by a ramp. There is a 1/d dependence in both cases.

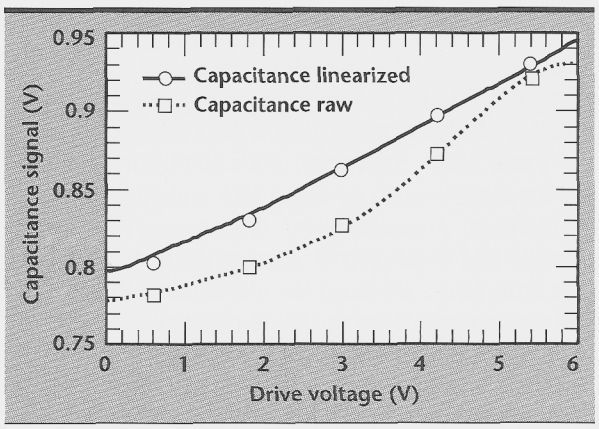


Figure 2. Capacitance signal as the micro-mirror is driven over a distance of 1200 nm.

MOSIS CMOS Chip

MOSIS is an electronic chip foundry that has specialized CMOS processes that range from sub-µm to 2-µm gate lengths. The advantage to using such a foundry is that the CMOS process is well-maintained and characterized. The second advantage is price. For small volume, the total fabrication cost for research chips is $600. The prices vary with size and processing requirements, but the cost is kept low by sharing the same silicon wafer with other users from around the country. Third, MOSIS runs on a set schedule, with delivery times as short as two months.

A second generation of the capacitive sensor circuit was implemented at the chip level in CMOS. The CMOS chip, although not entirely identical to the circuit in **Fig. 1**, contained most of the components, including the high-speed amplifiers and detector. The filters are implemented off-chip at this time. The frequency was chosen as 455 kHz, to match readily available filters. Many operational amplifier designs have very little gain at this frequency. The amplifier design was similar to that described by Saether.[1] This particular design was implemented in 2-µm CMOS, and has gain to well beyond 10 MHz.

The goal was to have each amplifier achieve a voltage gain of at least 10 at 455 kHz. Higher gains would then be realized by a cascade of 10× gain blocks. The gain-setting resistors were implemented in polysilicon. Although resistor formation using polysilicon is not highly accurate, the actual process values were within 10% of design values, which was close enough for this application.

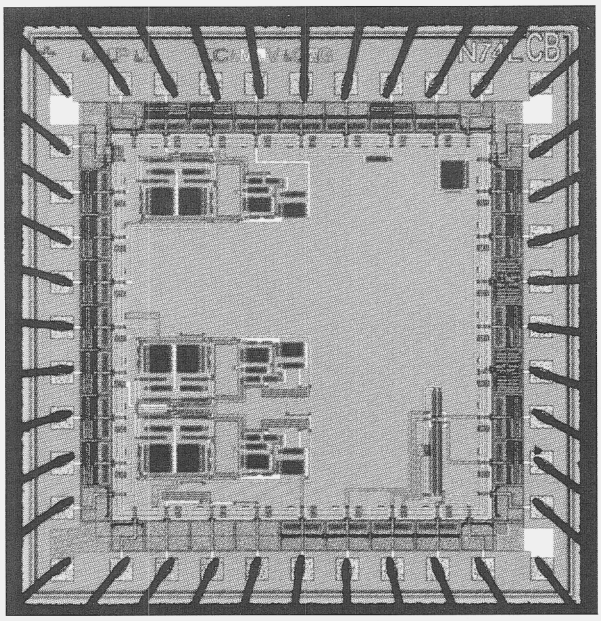


Figure 3. Photograph of MOSIS chip designed to measure capacitance position sensors in MEMS devices.

The circuit was designed using SPICE for circuit simulation. Actual model parameters for the n- and p-channel transistors were taken from the MOSIS data base of a previous 2-µm analog CMOS run. The actual layout was done using MATLAB on a Macintosh to generate the layouts for the various size transistors.

The MATLAB code generated all layers for each transistor. These layers consist of the n-well, polysilicon, active area, contact holes, two levels of metalization, and vias. The output of the MATLAB code was compatible with the KIC code which was used for layout. KIC is a UNIX code that resides on the LLNL Engineering computer TRINITY, and was used to manually place the MATLAB-generated cells, as well as manually route the on-chip wiring. The KIC output was converted to CIF format and sent electronically to MOSIS. The submission process is highly streamlined and tuned, since MOSIS has been doing this work for a number of years.

Figure 3a shows a picture of the completed chip. This chip had three amplifiers, a synchronous detector, and some test structures. A comparison of simulated and measured gain of the amplifiers is shown in **Fig. 4**. The frequency response is quite close to the prediction. The gain of the two-stage amplifier was supposed to be 40 dB, but was closer to 31 dB, because of some additional resistance in the input structure for the first amplifier. This is now understood and can be easily changed on the next iteration. The closeness of the modeled results gives confidence that more ambitious designs can be handled in the future.

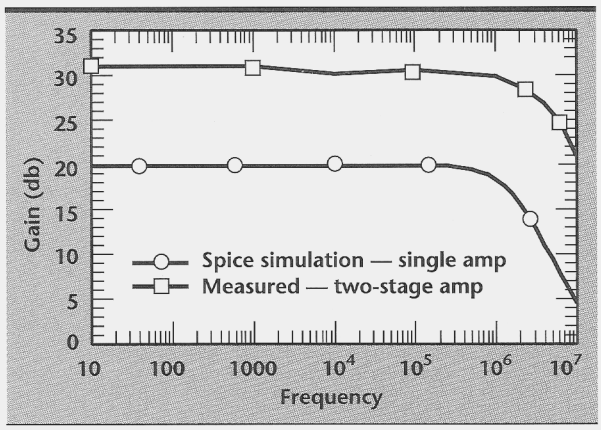


Figure 4. Comparison of measured gain vs frequency for a two-stage amplifier fabricated by MOSIS, with a simulation of the single-stage version. The predicted and measured frequency responses are quite close.

Future Work

At this time the current chips are wire-bonded. It is planned that some flip-chip techniques can be used in the future for mating these with the MEMS devices. It is also planned that other types of chips will be fabricated in the coming year to support new MEMS projects in wireless sensors, as well as existing projects in gas chromatography.

Acknowledgment

We would like to acknowledge D. Hadley for the layout and construction of the surface mount electronics for the capacitive sense electronics.

Reference

1. Saether, T., C. Hung, Z. Qi, M. Ismail, and O. Aaserud (1996), "High Speed, High Linearity CMOS Buffer Amplifier," *IEEE Jour. Solid-State Circuits*, Vol. **31**, (2), Feb., pp. 255–258.

Monolithic High-Performance Three-Dimensional Coil Inductors for Wireless Communication Applications

Vincent Malba
Engineering Research Division
Electronics Engineering

Anthony F. Bernhardt
Physics and Space Technology Directorate

Darrin J. Young, Jia-Jiunn Ou, and Bernhard E. Boser
Department of Electrical Engineering and Computer Sciences
University of California, Berkeley, California

An on-chip 3-D RF coil inductor is proposed as a key component to implement monolithic wireless transceivers. The device achieves a substantially superior performance compared to conventional spiral inductors, and is amenable to monolithic integration in a standard IC process, due to its low thermal budget. Experimental devices fabricated on a standard silicon substrate (10 Ω-cm) achieve a 2.6-nH inductance with a peak quality-factor (Q) of 13 at 900 MHz. The Q-factor is limited by a lossy adhesive used in the fabrication. In a modified process without adhesive in the coil area, a 4.8-nH inductor achieves a peak Q-value of 30 at 1 GHz. High-Q inductors with 8 nH and 13.8 nH have also been fabricated.

Introduction

Increasing demands for wireless communications motivate a growing interest in low-cost, monolithic personal communication transceivers. High-performance RF inductors are the key components for implementing critical building blocks, such as low-noise RF voltage-controlled oscillators (VCOs), low-loss impedance-matching networks, passive filters, and inductive loads for power amplifiers. Critical parameters include inductance value, quality factor (Q), and self-resonant frequency.

Many cellular communication systems, such as AMPS and GSM, operate around 1 GHz and require inductance values on the order of 5 nH, Q of at least 10, and a self-resonant frequency well in excess of the operating frequency. However, such high-performance inductors are not available in current silicon IC technology. Therefore, the integration of these devices has become the key task for realizing monolithic wireless transceivers.

Conventional aluminum spiral inductors fabricated on standard silicon substrates achieve Q-factors around 3 at 1 GHz.[1,2] Two issues contribute to the limited Q-factor: eddy currents in the substrate and metal resistive losses. The first problem can be addressed in part by removing the silicon substrate underneath the inductor, leading to a Q of around 5,[3] or a Q close to 10 at 1 GHz by using copper traces on a sapphire substrate.[4] While improving the Q-value, sapphire substrates are incompatible with standard IC processes.

Progress

In this paper, a new solution, based on a 3-D coil inductor is proposed. The 3-D micro-structure minimizes the device capacitive coupling to the substrate and eddy current loss. Thick copper traces reduce the series resistance, thus ensuring a high Q. Because of the low processing temperature, the inductor can be fabricated on top of wafers with completed electronics without affecting the characteristics of active devices. This is particularly crucial in RF applications, where the availability of the most recent IC technology is a critical competitive advantage.

Monolithic 3-D Coil Inductor

Figure 1 shows the schematic top and cross-sectional views of a 3-D two-turn coil inductor. The device consists of 5-µm-thick copper traces electroplated around an insulating core with a 650-µm × 500-µm cross-section. Compared to spiral inductors, this geometry minimizes the coil area that is in close proximity to the substrate, and hence minimizes the eddy current loss, resulting in a maximized Q-factor and self-resonant frequency of the device.

Copper is selected as the interconnect metal because of its low sheet resistance, critical for achieving a high Q-factor. The skin depth at 1 GHz determines the optimal metal thickness of 5 µm. The 50-µm metal width represents a compromise between the interconnect resistance and capacitance to the substrate. A 50-µm line spacing is used in this conservative design to avoid processing difficulties.

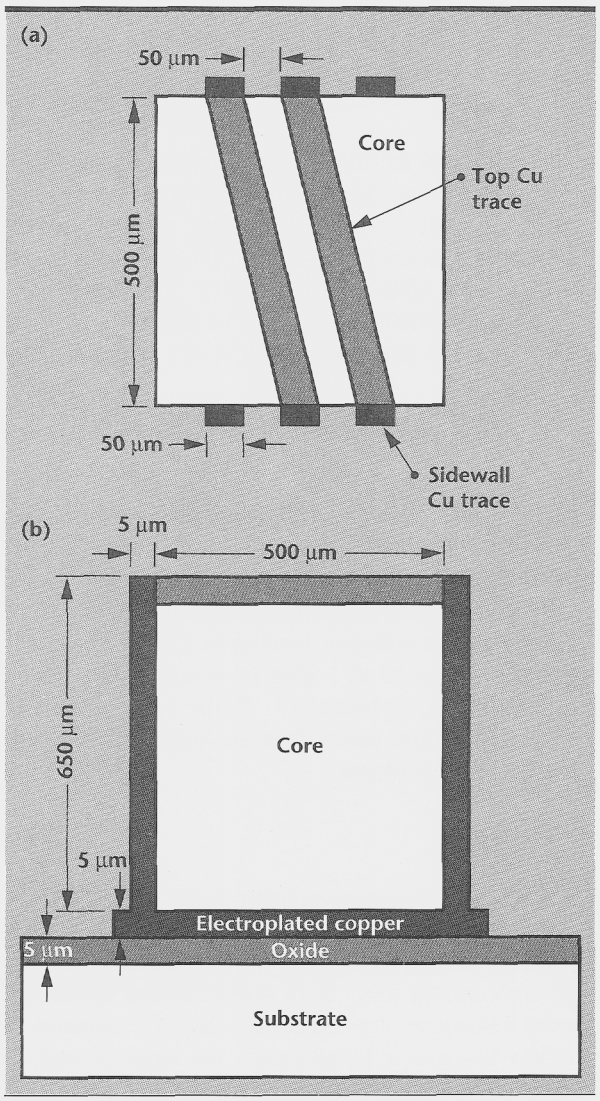


Figure 1. Schematic of 3-D coil inductor, showing (a) top view, and (b) cross-sectional view.

Alumina is used as the core material because of its negligible loss tangent at high frequencies,[5] a key parameter to ensure a high Q-factor. The core width of 500 µm is found experimentally to be the minimum that avoids tilting during attachment to the bottom copper traces. Its height is limited by the thickness of a commercially available alumina sheet.

A typical RF transceiver uses inductances on the order of 5 nH. For the current fabrication, devices with one, two, and four turns are designed to achieve 5 nH, 8.5 nH, and 13.5 nH, respectively.

Fabrication Process

Figure 2 illustrates the process flow. First, the wafers are passivated with 5-µm or 10-µm low-temperature oxide (**Fig. 2a**). Then the bottom traces of the inductors are fabricated. For this purpose, 50-nm titanium and 300-nm copper seed layers are sputtered and covered by an 8-µm-thick electroplated resist. The electroplating method is chosen because it can conformally deposit a thick resist on a complex surface such as an inductor core.

The patterns of the bottom metal traces are transferred photolithographically (**Fig. 2b**). This step is followed by selective electroplating of the 5-µm copper traces. To prevent oxidation, the copper is passivated with two 100-nm layers of electrolytic nickel and gold (**Fig. 2c**). Finally, the photoresist and copper/titanium seed layer are removed with a wet etch, leaving the bottom metal traces of the inductor on the substrate (**Fig. 2d**).

The core of the inductor is formed from an alumina sheet. The sheet is first covered with a 75-µm-thick electrically insulating thermoplastic adhesive film and then diced into 500-µm-wide strips. A 2% width accuracy has been achieved by using a thin diamond grit blade on a commercial dicing saw. The strips are then centered on the bottom copper traces and baked for 30 s at 170 °C to cure the adhesive (**Fig. 2e**).

To fabricate the copper traces on the side and the top of the alumina core, the same process is used as for the bottom traces (**Fig. 2f**). However, the resist is exposed with a 3-D maskless direct-write laser lithography tool.[6] After developing the laser-exposed resist, 5-µm-thick copper traces are electroplated at the sides and on the top of the alumina core. The completed inductor coil is illustrated in **Fig. 2g**.

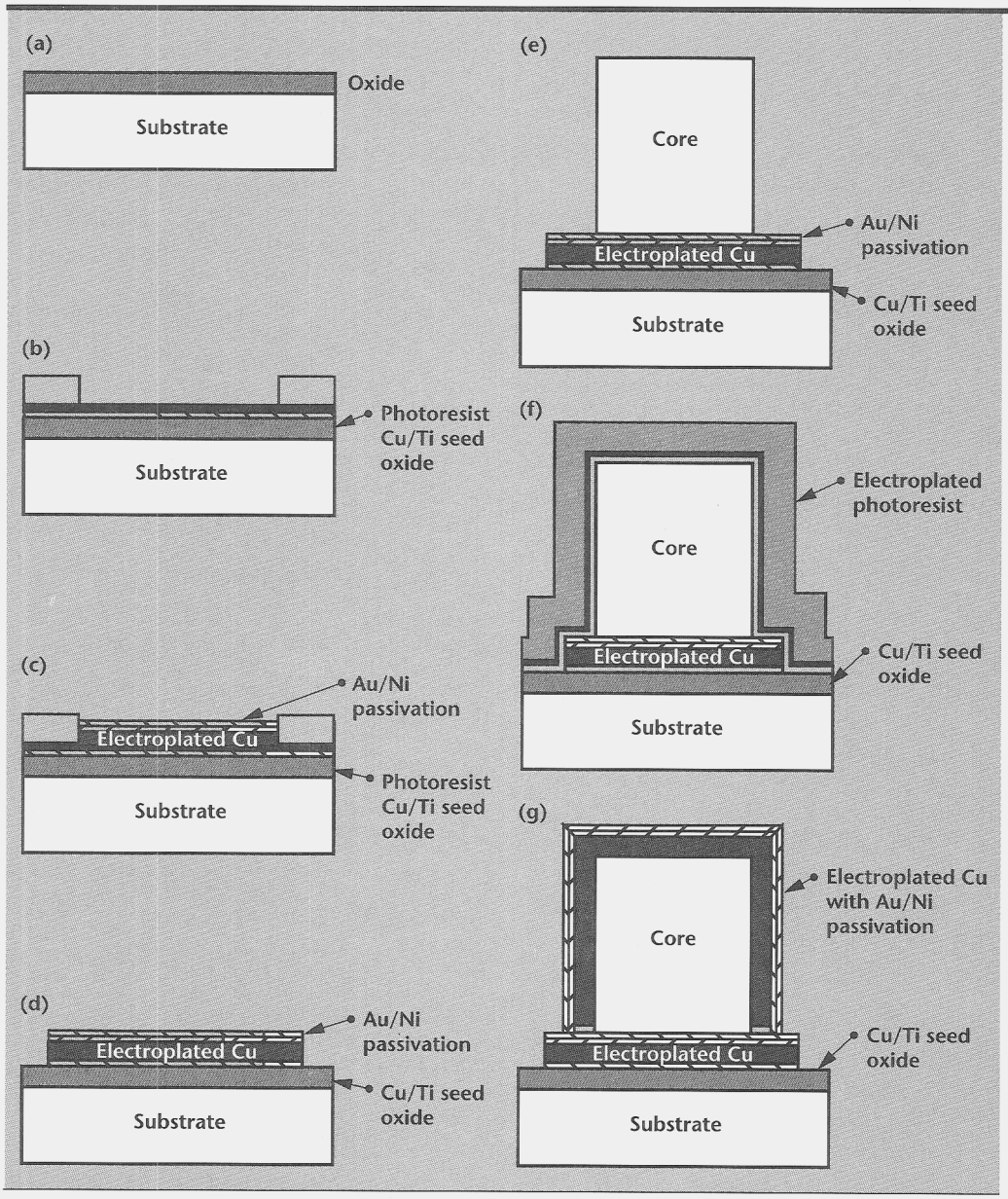


Figure 2. Fabrication process flow.

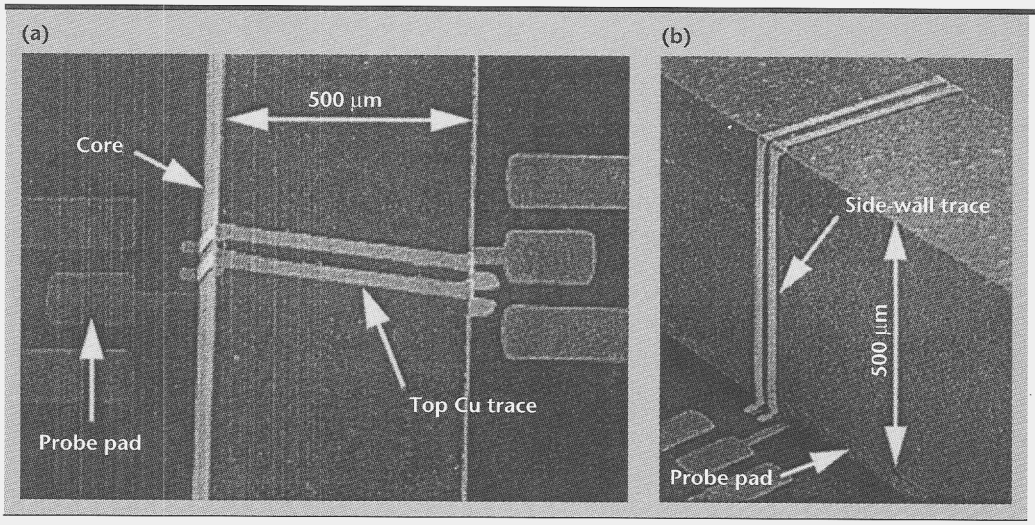


Figure 3. SEM of a two-turn coil inductor, showing (a) top view, and (b) side view.

Experimental Results

Figure 3 shows an SEM of a two-turn inductor on a standard silicon wafer with a 5-µm oxide layer above the substrate. The coil area above the substrate is approximately 250 µm × 500 µm, comparable to that of a typical spiral inductor of the same value.

The two-port S-parameters of the device are obtained with an HP8719 network analyzer. **Figure 4** shows the measured Q and the inductance value as a function of frequency after de-embedding the parasitics from the probe pads. The inductance is 2.6 nH, with a peak Q of 13 around 900 MHz. This Q-value is substantially higher than previous published results; however, the inductance is lower than the simulated value of 8.5 nH. Loss in the adhesive at high frequencies is suspected as the reason. This interpretation would also explain the rapid decrease of Q for frequencies above 1 GHz. A higher inductance (3.9 nH) is measured for inductors fabricated on a high-resistivity silicon substrate (1 kΩ-cm), but no improvement in Q at 1 GHz. Loss in the adhesive is again suspected as the reason.

Inductors recently fabricated with a modified process that does not use an adhesive inside the coil area achieve an improved performance. A two-turn inductor on a high-resistivity silicon substrate achieves 8 nH inductance with a Q of 16 at 900 MHz. These results closely match the simulated values. **Figure 5** presents an SEM of inductors with one and four turns.

Measurement results for these devices are shown in **Figs. 6** and **7**, and demonstrate a record Q of 30 at 1 GHz for a single turn device. The resonant frequencies for the devices are more than 4 GHz, well above the operating frequency of interest.

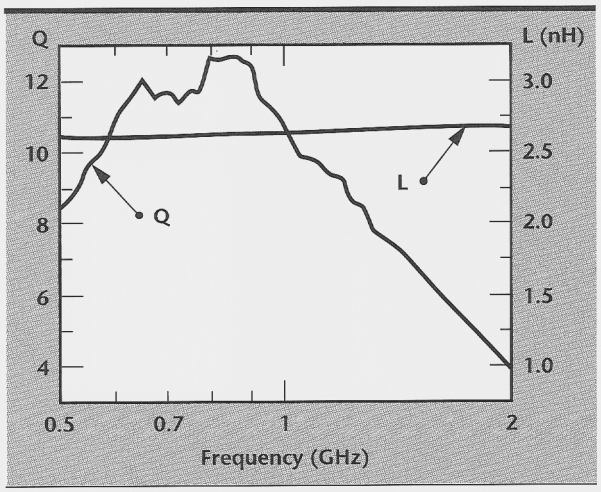


Figure 4. L and Q vs frequency for a two-turn inductor.

Conclusions

Compared to conventional aluminum spiral inductors, the proposed 3-D copper coil inductors achieve a substantially superior performance, with Q-values up to 30 at 1 GHz. These elements are critical for reducing the off-chip component count, lowering power dissipation, and improving the performance of personal RF communication devices such as cellular phones. While initial devices have been fabricated on bare silicon wafers, all fabrication steps are compatible with standard IC technology, thus allowing monolithic integration of active devices with high-Q inductors.

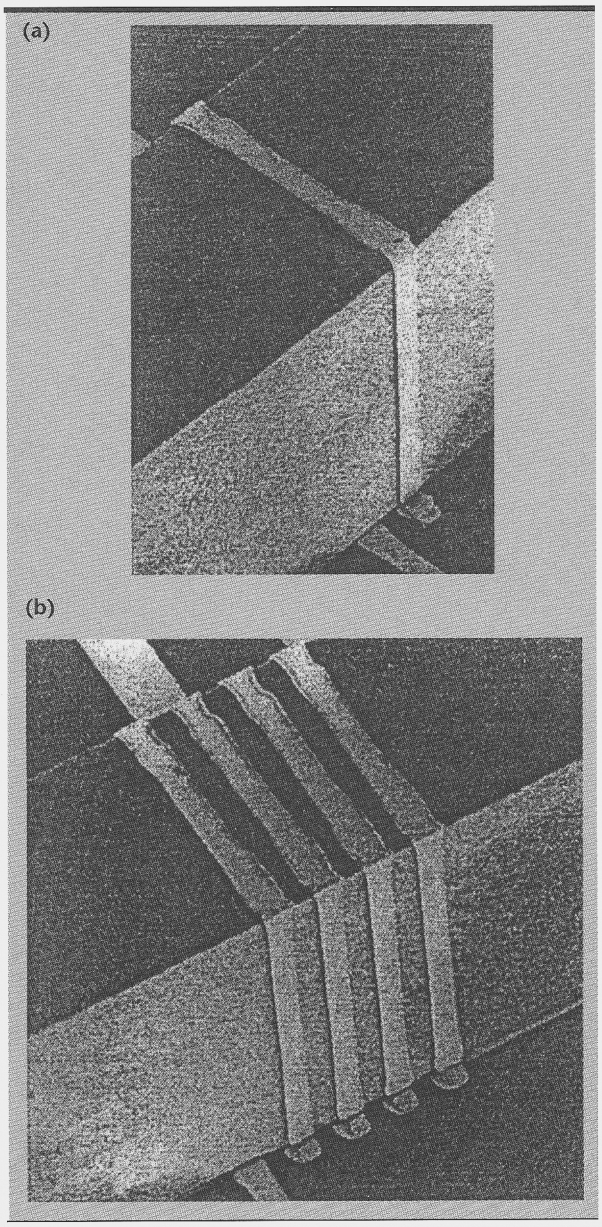


Figure 5. SEM of coil inductors: (a) one-turn inductor; (b) four-turn inductor.

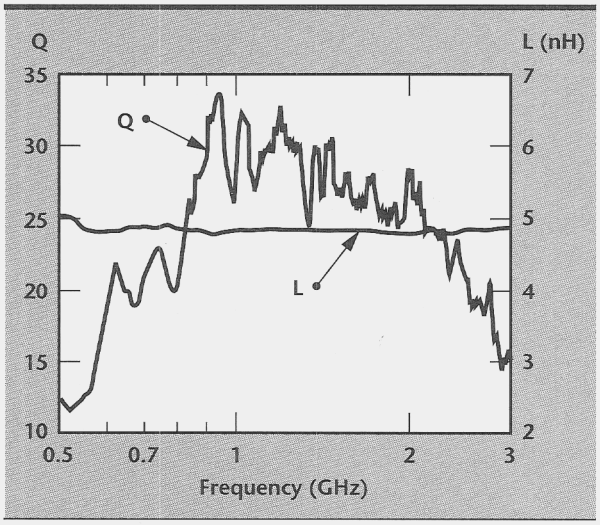


Figure 6. L and Q vs frequency for a one-turn inductor.

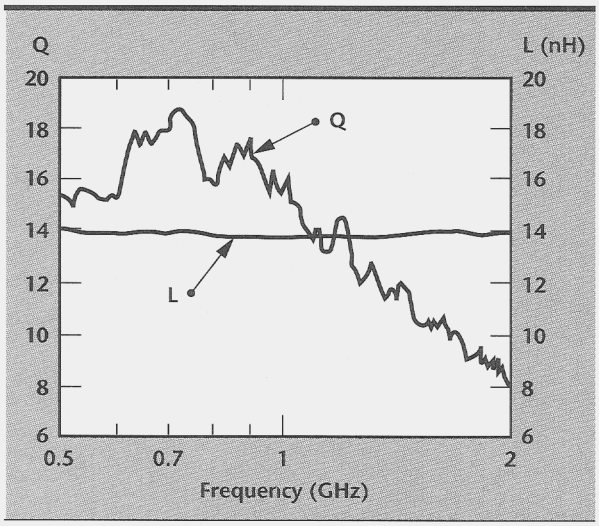


Figure 7. L and Q vs frequency for a four-turn inductor.

Acknowledgment

The authors wish to thank C. Harvey, L. Evans, and R. Graff for helpful suggestions and processing assistance. Certain fabrication steps were carried out in the University of California, Berkeley, Microfabrication Laboratory.

References

1. Nguyen, N. M, and R. G. Meyer (1990), "Si IC-compatible inductors and LC passive filters," *IEEE Journal of Solid-State Circuits,* August, Vol. **25**, (4), pp. 1028–1031.

2. Burghartz, J. N., M. Soyuer, and K. A. Jenkins (1996), "Microwave inductors and capacitors in standard multilevel interconnect silicon technology," *IEEE Transactions on Microwave Theory and Techniques,* January, Vol. **44**, (1), pp. 100–104.

3. Chang, J. Y-C., A. A. Abidi, and M. Gaitan (1993), "Large suspended inductors on silicon and their use in a 2-µm CMOS RF amplifier," *IEEE Transactions on Electron Device Letters,* May, Vol. **14**, (5), pp. 246–248.

4. Burghartz, J. N., B. C. Edelstein, K. A. Jenkens, and C. Jahnes (1996), "Monolithic spiral inductors fabricated using a VLSI Cu-damascene interconnect technology and low-loss substrate," *IEDM Tech. Dig.,* pp. 96–99.

5. Nakayama, A., and K. Shimizu (1994), "An improved reflection wave method for measurement of complex permittivity at 100 MHz - 1 GHz," *IECE Transactions Electron,* April, Vol. **E77-C**, (4), pp. 633–638.

6. Malba, V., V. Liberman, and A. F. Bernhardt (1997), "Fabrication of a DRAM cube using a novel laser patterned 3-D interconnect process," *Proceedings of the International Conference on Multichip Modules,* April, pp. 160–165.

Vertical-Lasing Semiconductor Optical Amplifiers

Jeffrey D. Walker and Sol P. DiJaili
Engineering Research Division
Electronics Engineering

We have established the design, growth, and fabrication of the first vertical-cavity laser diodes developed at Lawrence Livermore National Laboratory (LLNL). These lasers, the first single-mode vertical-lasing amplifiers ever built, were used to demonstrate gain-clamped vertical-lasing semiconductor optical amplifiers that operated at a wavelength of 0.85 µm. They have a chip gain of 17 dB, and a threshold current of 100 mA, which is a factor of four lower than previously demonstrated devices.

Introduction

Optical amplifiers are used to make up for propagation and splitting losses in fiber-optic networks. They can provide an optical gain on the order of 30 dB; in other words, they can boost the intensity of light traveling through them one thousand times.

There are two basic types of optical amplifiers, the erbium-doped fiber amplifier (EDFA), and the semiconductor optical amplifier (SOA). The SOA has many potential advantages over the EDFA, including size, cost, power, speed, and wavelength agility. However, the EDFA is now used in commercial systems because of problems that have existed with current SOA technology. The fundamental problem that has prevented the use of SOAs in commercial applications is cross-talk, which arises from gain variations in the amplifier and causes distortion of signals as they travel through the device.

The purpose of this project was to establish the usefulness of an LLNL-patented technology that solves the cross-talk problem in SOAs. The solution is to use a vertical-lasing field to clamp the gain in the SOA, and thereby eliminate the cross-talk problem. Previous proof-of-principle demonstrations of this vertical-lasing SOA (VLSOA) device showed the basic effect of cross-talk reduction in this structure.[1] However, the previous work had several deficiencies, including high operating current, a multi-mode SOA waveguide, and operation at the wrong wavelength for commercial applications. This report demonstrates the first low-operating-current, single-mode, 0.85-µm wavelength VLSOAs.

Progress

A sketch of the VLSOA is shown in **Fig. 1**. It is basically a long and narrow vertical-cavity surface-emitting laser (VCSEL) that lases vertically and amplifies laterally. VCSELs are a relatively new type of laser diode that emit light vertically out of the top of the semiconductor wafer, as compared to conventional laser diodes that emit light laterally out of the side of the wafer. Compared to conventional edge-emitting laser diodes, VCSELs are extremely complex and high-precision devices that are difficult to fabricate.

In the first phase of this project, we demonstrated the first VCSELs that were designed, grown and fabricated at LLNL. These VCSELs were designed to operate at a wavelength of 0.85 µm, and they are similar to those found in the literature,[2] except that the cavity region is expanded, and a graded index section is inserted to provide vertical

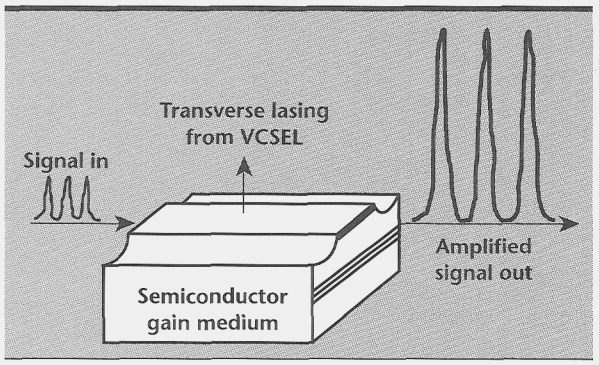


Figure 1. Sketch of VLSOA.

waveguiding for the SOA mode. The lasing threshold current for a 5-µm-×-200-µm device was 100 mA.

Once we established the capability to fabricate VCSELs, we were able to apply this technology toward development of a VLSOA. In this second generation VLSOA, we were able to demonstrate a single-mode device by adding single-mode vertical and lateral index confinement for the SOA mode. In the vertical direction, a conventional VCSEL is a poor waveguide because the average refractive index of the mirror is greater than that of the optical cavity. For this reason, the light traveling in the SOA would be expected to leak out of the cavity region and into the mirror cladding.

In the present structures, this problem was solved by extending the VCSEL cavity region to be a number of wavelengths thick, and adding a graded-index waveguide region around the quantum wells. In the lateral direction, waveguiding was achieved by reducing the waveguide width from 20 µm in the first generation devices down to 5 µm, and by maintaining a lateral index step on the order of 0.1%. Reduction in the width of the structure had the additional advantage of greatly reducing the threshold current of this second generation device.

To facilitate measurement, the gain of the VLSOA devices was determined by measuring the amplified spontaneous emission (ASE) power as a function of current.[3] **Figure 2** shows the gain vs current plot for a 200-µm-long second generation VLSOA structure. The data is collected with the device active side up, and without heat sinking. Because of the lack of adequate heat sinking, the device was operated pulsed, with a 1% duty cycle. Using this measurement technique, the gain shows the effects of clamping above 100 mA injection current. While the gain is not completely flat in the clamped region, this data differs greatly from that of a conventional SOA, for which the ASE power would be expected to continue to increase rapidly to a saturation point of typically 30 dB gain. The reason the gain is not completely flat is attributed either to unclamped regions along the waveguide where the VCSEL is not lasing, or to collection of stray ASE light generated outside of the SOA waveguide. From **Fig. 2**, the clamped chip gain of the VLSOA is about 17 dB. The threshold current for the gain clamping of 100 mA is four times lower than that of the first generation devices that have thresholds of 400 mA, for devices with similar chip gain.[1]

The VLSOA devices were fabricated with windows in the top VCSEL mirror to allow the observation of the VCSEL light during operation. **Figure 3** shows the overlapping VCSEL and SOA optical spectrum for the VLSOA of **Fig. 2**. This plot was generated by collecting the ASE light emitted from the SOA waveguide with a multi-mode fiber, and simultaneously collecting VCSEL light emitted vertically out of the top of the device with a second fiber. The two fibers were then combined with a fiber coupler and the data was observed using a Hewlett Packard optical spectrum analyzer. The data in **Fig. 3** was collected at 120 mA current injection in the gain-clamped region of operation. The reason the VCSEL spectrum does not go off-scale is that only a small fraction of the VCSEL power was collected.

The combined VCSEL/SOA spectrum, shown in **Fig. 3**, was used to observe the behavior of the

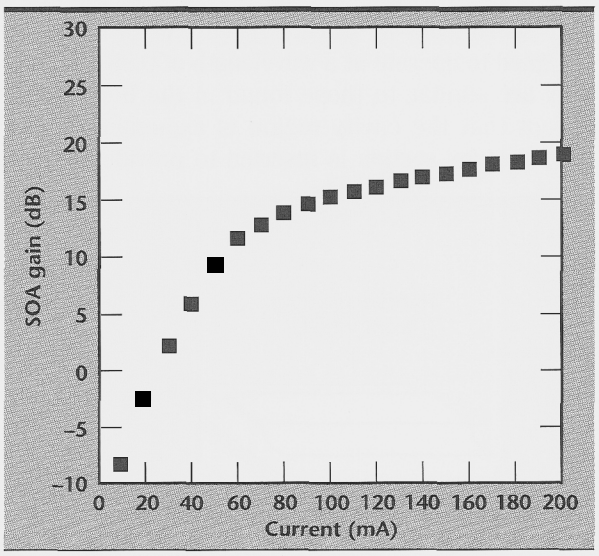


Figure 2. Gain as a function of current for a VLSOA device.

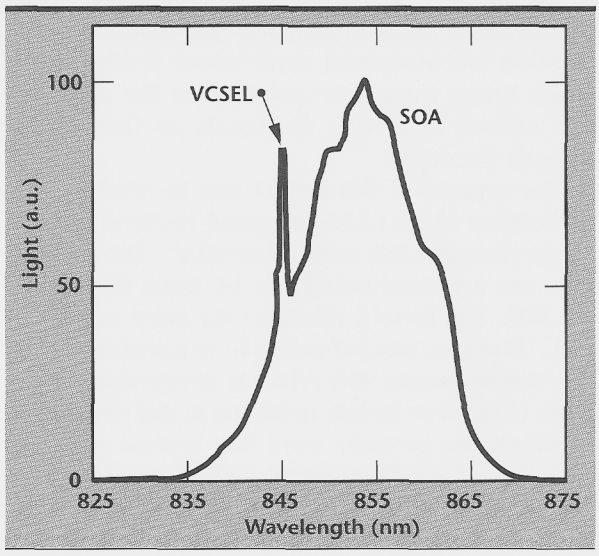


Figure 3. Combined VCSEL/SOA optical spectrum.

VLSOA device. As expected, as the injection current increased, the current at which the VCSEL begins to lase is consistent with the observation of gain clamping of the SOA. **Figure 3** also shows that in these devices, the VCSEL wavelength is blue-shifted from the peak of the gain spectrum. Because the gain medium is homogeneously broadened, the gain is expected to be clamped independent of the VCSEL wavelength. However, in future devices it may be desirable to move the VCSEL wavelength closer to the gain peak to further reduce the threshold current for gain clamping.

In summary, this work represents the first VCSELs fabricated at LLNL, the first single-mode VLSOA, the first 0.85-µm VLSOA, and the first low-threshold-current VLSOA. A gain-clamped amplifier was presented, with a chip gain of 17 dB, and a clamping threshold current of 100 mA. Additional work will be required to extend the operating wavelength to the communications wavelengths, 1.3 and 1.55 µm, and to further refine the design and fabrication of these devices.

Acknowledgments

The authors would like to acknowledge the diligent efforts of W. Goward, H. Petersen, and P. Stephan.

References

1. Walker, J. D., F. G. Patterson, S. P. DiJaili, and R. J. Deri (1996), "A gain-clamped, crosstalk free, vertical cavity lasing semiconductor optical amplifier for WDM applications," *Integrated Photonics Research Conference, Boston, MA*, **IWD1-1**, April 29–May 2.

2. Walker, J. D., D. M. Kuchta, and J. S. Smith (1991), "Vertical-cavity surface-emitting laser diodes fabricated by phase-locked epitaxy," *Appl. Phys. Lett.*, **59**, p. 2079.

3. DiJaili, S. P., J. D. Walker, F. G. Patterson, and R. J. Deri (1996), "Thermally robust optical semiconductor devices using AlGaInAs grown by molecular beam epitaxy," *LLNL Engineering Research, Development and Technology FY96 Thrust Area Report*, Lawrence Livermore National Laboratory, Livermore, CA, (UCRL 53868-96), **3**, pp. 29–33.

Field-Emission Cathode Micro-Electro-Mechanical System Technology for Sensors, Diagnostics, and Microelectronics

Jeffrey D. Morse, Jackson C. Koo, and Robert T. Graff
Electronics Engineering Technologies Division
Electronics Engineering

Alan F. Jankowski and Jeffrey P. Hayes
Materials Science and Technology Division
Chemistry and Materials Sciences

We have investigated field-emission devices for applications in sensors, diagnostics, and microelectronics. Field-emission devices micromachined from silicon and molybdenum have been fabricated and tested. Experimental results have shown that the presence of nitrogen gas molecules for pressures up to 1 mTorr has only a moderate impact on device emission performance, and has no long term effect on device operation. These results demonstrate that field-emission cathodes can potentially be used in sensors applications where gas ionization by electron impact is desirable, or other applications in which the field-emission device is exposed to less than ideal vacuum conditions.

Introduction

A substantial level of interest from Lawrence Livermore National Laboratory (LLNL) programs, government agencies, and the private sector has been generated to use miniature electron sources for a variety of applications, including ion gages, ion cells, cathodes for x-ray sources, and radiation hard microelectronics.

In most cases, a solid-state field-emission cold cathode would replace a thermionic emitter, or filament. Of these applications, several stand out as having significance for LLNL programs and Department of Energy (DOE) directives. These include radiation hard vacuum microelectronics; electron sources for miniature x-ray sources having remarkably small spot sizes for imaging, diagnostics, and instrumentation; field-emission cathodes (FECs) as an electron source for an ion cell in a portable mass spectrometer,[1] and as an ion cell detector for potential use in gas chromatography.[2]

The last application, which is the focus of this report, requires critical understanding of micro-electro-mechanical (MEMs) systems design, along with integration of field-emission devices, to realize a new micro-sensor technology. The advantage is that a low cost, micro-miniature, gas-molecule detector sub-system technology can be realized, with improved sensitivity over existing detectors. Furthermore, this ion cell can be integrated for specific application to gas chromatography systems. This technology would support industrial and environmental programs for the monitoring of toxics, pesticides, and petroleum products. In these applications parts-per-billion sensitivity is required in compact, portable systems.

At present gas-molecule detection schemes consist of several approaches, including helium ionization detection (HID), electron capture detection (ECD), both of which are highly sensitive (many parts per billion), and thermal conductivity detectors (TCD), with sensitivity limited to a few parts per million.

The ECD is more selective, being limited to sample molecules having sufficient electron capture cross-sections, such as pesticides and PCBs. ECDs therefore are useful in environmental monitoring applications. HIDs are more universal in the range of gas sample molecules that can be detected. This system implements a windowless photo-ionization system in which a carrier gas (helium or doped helium) is ionized by pulsed discharge. The UV

radiation then propagates to the detection region where it ionizes the sample gas without exciting the carrier gas. The free electrons are then collected by an electrode with a current peak corresponding to the sample molecule. Presently, these high sensitivity detection systems suffer from the need for a pulse discharge or radioactive source to generate ionizing UV radiation.

Unfortunately, these approaches are neither desirable nor conducive to micro-miniaturization, low cost, and high performance.

Progress

Gated field-emission, cold-cathode electron sources were evaluated as an improved means to generate electrons that could subsequently be used as an ionization source. The concept is illustrated in **Fig. 1**. Field-emission devices are cathode structures that are formed to atomically sharp tips which are in the proximity of an extraction, or gate electrode. By applying a positive voltage to the gate electrode with respect to the cathode, electrons are emitted into the vacuum above the gate, where they are swept away by the anode electric field. The efficiency of the field-emission process depends on the gate-to-tip spacing, the shape of the tip, and the effective work function of the tip material.

The potential advantages of field-emission devices as an electron source are improved efficiency, addressability and control, no heating of surrounding areas, and faster turn-on. Furthermore, field emitters are made using standard microfabrication processes, thus are more conducive to implementation into arrays, specific cathode designs, and integration with other microfabricated components.

These advantages can impact the performance of an ionization source in several ways. First, the FEC is controlled by a gate electrode, therefore is electrically addressable, and uses only a fraction of the power of filaments or pulse discharge electrodes. Field-emission devices can be integrated within the gas microflow system to directly ionize the sample gas, or be used in a manner to generate UV photons by ionizing a carrier gas, such as helium. The UV photons subsequently ionize the sample gas molecules. Thus, field emitters enable more flexibility and lower power usage in the ionization and detection scheme.

An FEC array was designed having an active emission area ranging from 25 μm × 100 μm (800 emitters) to 100 μm × 200 μm (10,000 emitters). **Figure 2** illustrates the fabrication sequence for making a gated FEC device using the Spindt cathode technique.[3–5] Using a proprietary lithographic technique developed at LLNL, gate-to-tip spacings of <0.1 μm have been achieved, as illustrated in **Fig. 3**. Process development consisted of several iterations of this sequence to optimize problems associated with adhesion of thin films, uniformity of emitters, gate hole diameter, pattern transfer, and gate-to-cathode leakage current. While most of these issues have been addressed and resolved, the issue of gate leakage current remains problematic.

A vacuum test station has been assembled to characterize the FECs at pressures on the order of 10^{-7} Torr. The test apparatus includes a fixture on which the FEC is mounted and electrical leads attached. The anode is then positioned to within 0.5 mm of the cathode array to collect any electrons that are emitted. Vacuum testing of these devices has demonstrated field-emission current turn-on with less than 50 V applied to the gate electrode.

As previously mentioned, a limitation of devices fabricated is the excessive gate leakage current

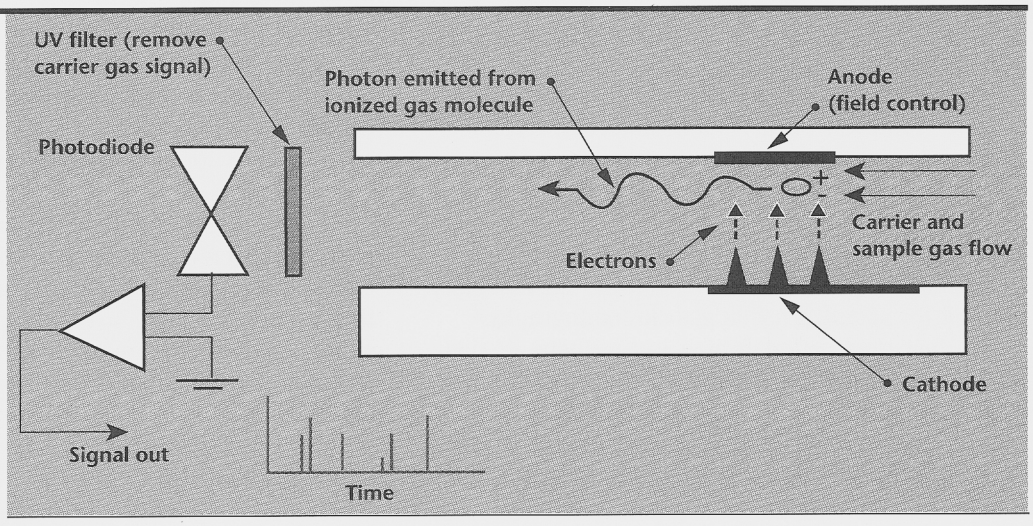


Figure 1. Schematic of ion cell concept with integrated field-emission devices.

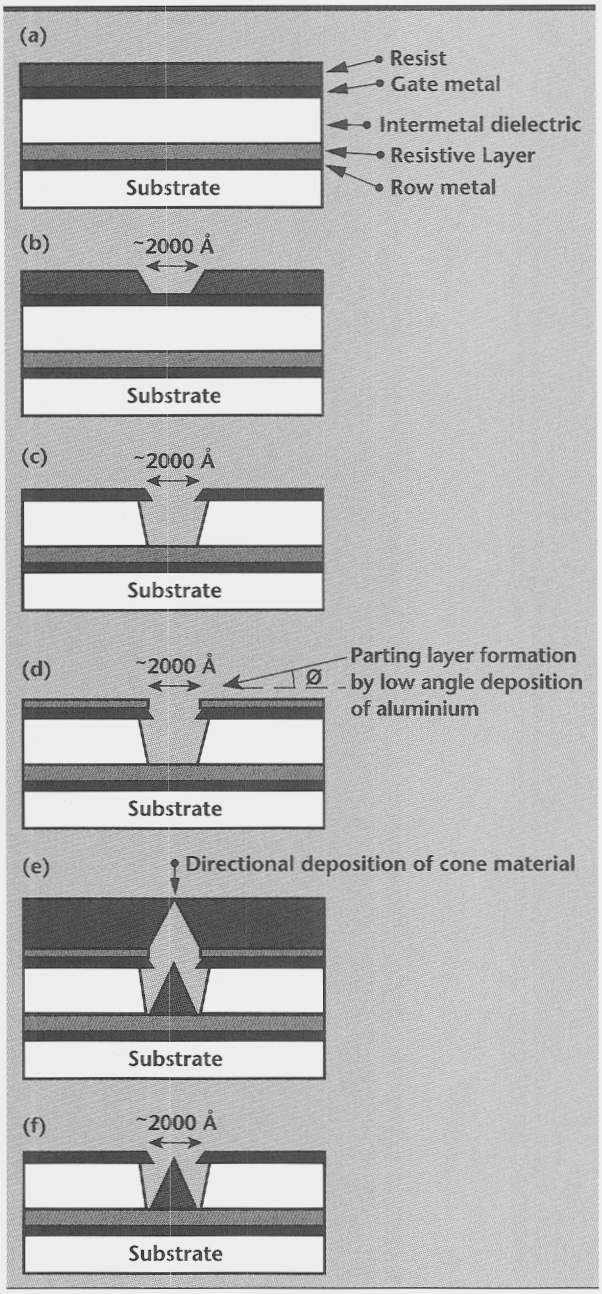


Figure 2. Cross-sectional schematic diagram of field-emission cathode fabrication process sequence: a) initial stack of thin film layer with resist deposited on top; b) patterning of resist by lithographic techniques to form gate structure; c) etching of the gate metal through the mask and the cavity in the intermetal dielectric; d) field-emitter tips formed by depositing a parting layer; and e) directional deposition of the tip material. The final emitter structure (f) is formed after lifting the parting layer from the gate metal.

which is orders of magnitude greater than the emission current, as illustrated in **Fig. 4**. This problem is being addressed, and is likely a result of contamination in the intermetal dielectric, or metal, shorting the tip directly to the gate electrode. Further iterations should resolve this problem. The impact on

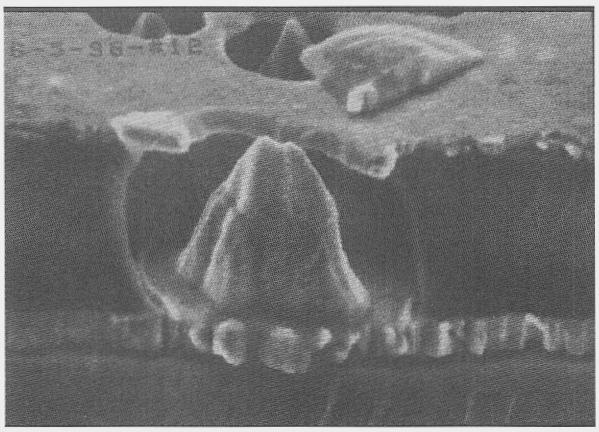


Figure 3. Gated field-emission cathode fabricated using sequence shown in Figure 1. Gate diameter for this device is 2000 Å.

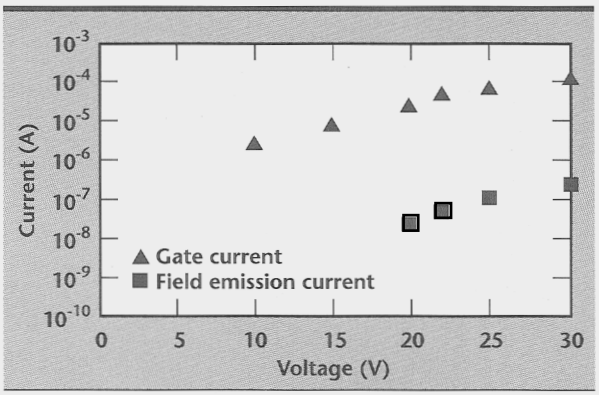


Figure 4. Current/voltage characteristics for field-emission cathode array. Current, measured at anode with 1.5 kV applied, and gate electrode, are illustrated as a function of gate-to-cathode voltage.

device performance is that the FEC will burn out when the gate current reaches some value, on the order of 100 µA, thus limiting the field-emission current to about 50 nA. Other solutions to this problem include an integrated ballast resistor, which in effect will minimize the impact of shorting due to point defects.

Arrays of ungated, silicon field emitters were fabricated and tested. The silicon tips were created by patterning a silicon nitride mask on heavily doped, n-type silicon. The silicon was then isotropically etched, undercutting the nitride mask, until the silicon formed a relatively sharp point. The silicon tip arrays are illustrated in **Fig. 5**.

The silicon field-emitter array was mounted on the test fixture, and positioned in the vacuum test chamber, with an anode spacing of approximately 500 µm above the tips. Field-emission current was then monitored as the anode voltage was increased. These characteristics were monitored as the pressure was increased by introducing nitrogen to the chamber.

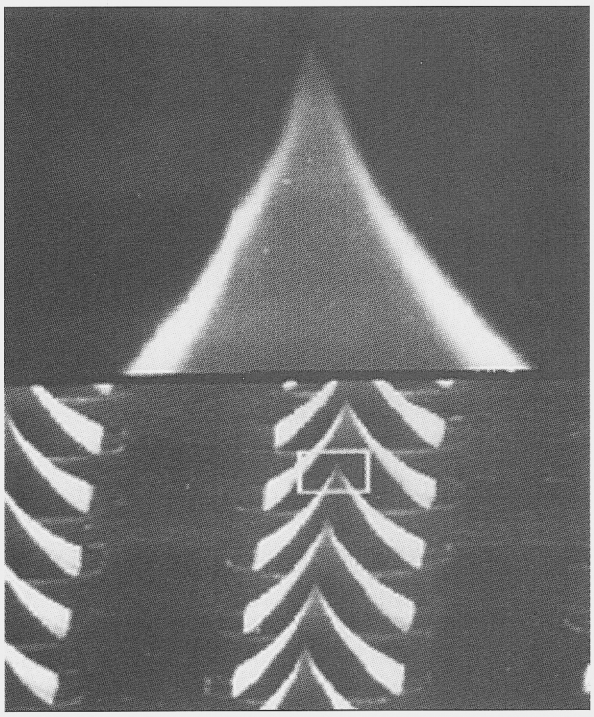


Figure 5. Scanning electron micrograph of silicon field-emission tip arrays.

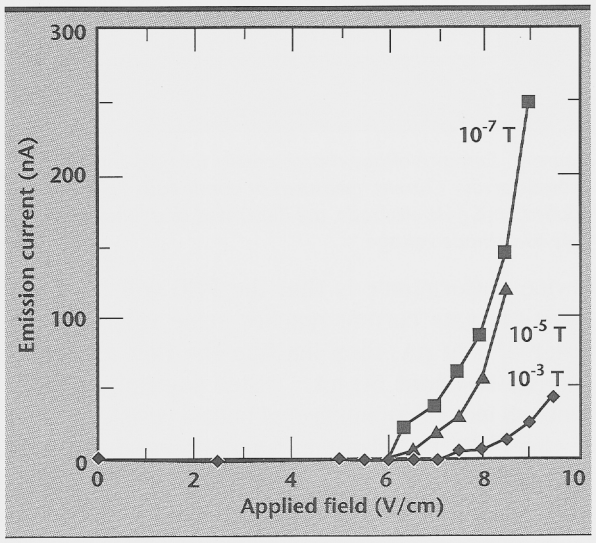


Figure 6. Experimentally measured current/voltage characteristics of silicon field-emitter tip array with varying nitrogen pressure.

The performance of the silicon emitter array at various pressures is illustrated in **Fig. 6**. We observed that the relative field-emission current decreases at higher pressures, likely resulting from increased scattering of the emitted electrons with the gas molecules. Upon further inspection of the silicon tip array after testing, we observed no physical damage to the devices.

Future Work

Ionization sources are finding increased uses for a variety of applications. Efforts to further evaluate the performance of field-emission devices in non-ideal vacuum, and higher gas flow conditions are continuing, to understand the optimal design and performance for this application. Once completely evaluated, field-emission devices can be integrated with microflow components, to realize a MEMS-based micro-analytical instrument for detection and identification of trace chemical species.

References

1. Spindt, C. A. (1992), "Microfabricated field-emission and field-ionization sources," *Surface Science,* North Holland, **266**, pp. 145–154.

2. Snyder, A. P., C. S. Harden, A. H. Brittain, M-G. Kim, N. S. Arnold, and H. L. C. Meuzelaar (1996), "Portable Hand-held Gas Chromatography/Ion Mobility Spectrometry Device," *Analytical Chemistry,* February, Vol. **65**, (3), pp. 299–306.

3. Spindt, C. A., I. Brodie, L. Humphrey, and E. R. Westerberg (1976), "Physical properties of thin-film field-emission cathodes with molybdenum codes," *J. Appl. Phys.,* **47** (12), p. 5248.

4. Spindt, C. A., C. E. Holland, P. R. Schwoebel, and I. Brodie (1996), "Field-Emitter-Array Development for Microwave Applications," *J. Vac. Sci. Technol. B,* **14** (3), p. 1986.

5. Bozler, C. O., C. T. Harris, S. Rabe, D. D. Rathman, and M. A. Hollis (1994), "Arrays of Gated Field-Emitter Cones Having 0.32-µm Tip-To-Tip Spacing," *J. Vac. Sci. Technol. B,* **12** (2), p. 629.

Blue Laser Diode Process Development

Glenn A. Meyer
New Technologies Engineering Division
Mechanical Engineering

Gregory A. Cooper and Stacy L. Lehew
Electronics Engineering Technologies Division
Electronics Engineering

Steven DenBaars
Photonics Group
University of California, Santa Barbara

We have developed a dry etching process for fabricating optical quality laser mirrors with parallel facets on gallium nitride (GaN)-based materials. The process uses a chemically-assisted ion beam etching technique, with a Xe-ion beam and chlorine gas (Cl_2). Laser mirrors dry etched at Lawrence Livermore National Laboratory (LLNL) on an InGaN/GaN laser device grown at the University of California, Santa Barbara (UCSB) recently demonstrated lasing under pulsed power at room temperature, emitting at a wavelength of 419 nm.

Introduction

Semiconductor laser diodes have found widespread use in many commercial applications owing to their small size, high efficiency, low cost, and high reliability. While reliable and efficient semiconductor lasers presently operate in the visible (630 nm) to IR (2000 nm) wavelength range, it has proved to be considerably more challenging to demonstrate useful laser diodes at shorter wavelengths. The ability to produce green, blue, and near-ultraviolet laser diodes would allow full color displays, and would enable very high-density optical memory storage for CD-ROMs.

Currently, lasers that read data in CD players use gallium arsenide (GaAs) diodes which emit red light at a wavelength of 780 nm. The readable data density could be increased by a factor of four if the spot size is reduced using shorter wavelength blue laser diodes, emitting light in the 460 nm wavelength range. High-power laser diodes in this wavelength range would also allow new laser diode-pumped solid-state laser systems to be realized.

The Ti:sapphire laser is a widely used solid state laser because of its wide tuning range, from 670 nm to 1070 nm, and its ability to generate femtosecond pulses. However, the short pump wavelength of this material involves the use of a separate laser to generate the required pump intensity. This is usually done with large Ar-ion lasers, or frequency doubled Nd:YAG or Nd:YLF lasers. A laser diode-pumped tunable Ti:sapphire laser would eliminate the need for a separate pump laser module. Blue laser diodes would also eliminate the need for frequency doubling crystals in certain systems, thus reducing laser system complexity, enhancing reliability and boosting efficiency.

Blue laser diodes could find applications in a host of areas as diverse as information storage, RGB displays, submarine communications, bio-warfare detection systems, materials processing, biotechnology, and laser surgery. They can also be pump sources for new solid state and dye laser systems.

Light emitting diodes (LEDs) are much simpler devices to fabricate than laser diodes. The light emitting structure of the two devices is similar where light is emitted at the junction between n-type and p-type semiconducting materials. In LEDs, the light that is generated at the junction passes through the transparent semiconductor layers and leaves the device. In laser diodes, some of the light is reflected by mirrors back into the light generating

region and is amplified. The mirrors are fabricated out of the semiconductor diode material itself. The intensity of light emitted from a laser diode is much higher than that emitted from an LED.

Several years ago the first blue-green LEDs were produced using ZnCdSe-based materials. Unfortunately, their reliability is intrinsically poor, and it is unlikely that this system will ever produce the requisite commercial/military lifetimes (> 10,000 h of operation).

Alternatively, there has been considerable progress in the AlGaInN material system. AlGaInN exhibits high thermal conductivity and thermal stability, and covers the wavelength range of 250 to 600 nm. The progress has been so compelling that commercial blue GaN LEDs have already replaced blue SiC LEDs, due to their higher brightness and efficiency. It is expected that the conventional yellow/green LEDs may soon be replaced as well.

At UCSB multiple quantum well (MQW) InGaN LEDs have also been fabricated, and emit bright blue to green direct-gap luminescence peak wavelengths of 450 nm and 550 nm. The luminescence peaked at 450 nm and the external quantum efficiency was 4.5% for the MQW structure at 20 mA.[1] High peak power output of 55 mW was measured under a pulsed condition of 1 A, for 3 µs pulse width, which is almost twice as bright as commercially available LEDs from Nichia Chemicals Ltd., Japan.

In 1996, S. Nakamura at Nichia, demonstrated the first current injection InGaN/AlGaN laser diode, emitting at 417 nm.[2] S. Nakamura has now achieved lifetimes of more than 1000 h for an InGaN MQW structure laser diode emitting at 390 to 440 nm, operating CW at room temperature.[3] In 1997 M. Mack, A., and Abare S. DenBaars succeeded in growing, fabricating, and testing a current injection InGaN/GaN laser diode, thus making UCSB the first university to demonstrate a 419-nm blue laser diode at room temperature.[4] The UCSB laser diode consisted of a 10-InGaN-MQW active region grown on c-plane sapphire substrates with uncoated reactive ion etched (RIE) facets.

Under pulsed operation, lifetimes exceeding 6 h have been demonstrated with peak powers as high as 17.6 mW and threshold current densities as low as 12.7 kA/cm^2. To date, only eight research groups in the world have produced blue, current injection GaN laser diodes: Nichia, Fujitsu, Toshiba, Cree, USCB, Sony, Xerox, and HP/Meijo University.

One important step in the manufacture of laser diodes or advanced electro-optic devices is the fabrication of mirrors that provide the optical feedback necessary for lasing. Mirrors for laser applications require vertical, smooth sidewalls. Although high-quality laser mirrors in conventional laser diode material (cubic GaAs) can be fabricated by cleaving on the {100} crystal planes, this method does not work well with the hexagonal crystal structure of GaN. It is thus necessary to develop other methods to fabricate the laser mirrors for GaN.

Dry etching techniques have been perfected at LLNL, and by several other research groups around the world, to produce facets and mirrors on GaAs opto-electronic devices. These processes use an ionized reactant to remove material from the surface of the device by a combination of chemical and/or mechanical processes. The chemically-assisted ion beam etching (CAIBE) technique has become the dominant technique to fabricate facets and mirrors on opto-electronic devices in AlGaAs/GaAs heterostructures.[5,6]

Other researchers using RIE, electron cyclotron resonance discharge, and CAIBE have demonstrated effective etching of GaN. One group[7] achieved GaN etch rates of greater than 50 nm/min by RIE in silicontetrachloride plasmas ($SiCl_4$, 1:1/$SiCl_4$,:Ar, and 1:1/$SiCl_4$:SiF_4) at a bias voltage of 400 V. However, over-cut etching of the sidewall, which resulted in tapered sidewalls, was observed.

CAIBE of GaN using an argon ion beam in hydrogen chloride gas (HCl)[8] and Cl_2[9] shows promise as a method to fabricate laser facets and mirrors. Near-vertical sidewall profiles were achieved on GaN using an Ar-ion beam energy of 500 eV at 0.9 mA/cm^2 under flowing HCl at 10 sccm at 300 °C.[8] Etch rates as high as 210 nm/min have been observed. However, the GaN etch surface following CAIBE in both Cl_2 and HCl at elevated temperatures of 300 °C was roughened and decorated with round "potholes."

At lower temperatures of 20 °C, smoother surfaces were observed with comparable etch rates but the sidewalls were slightly sloped.[9] One group[10] reported similar roughened $In_{0.5}Ga_{0.5}N$ surface morphology following Cl_2 etching using the electron cyclotron resonance (ECR) discharge technique. By adding sulfur hexafluoride (SF_6) or H_2 to the Cl_2 discharge, smoother surface morphologies were obtained. It was suggested[10] that with increasing H_2 or SF_6 concentrations in a Cl_2 discharge, the N atoms are more efficiently removed from the sample surface. Since H_2 is known to passivate dopants in other semiconductor devices,[11] the Cl_2/SF_6 chemistries may have an advantage over H_2/SF_6 chemistries, due to the absence of H_2.

The objective of this project is to develop a dry etching process for the fabrication of optical quality laser mirrors in GaN-based laser diode devices.

This requires parallel (90°) laser mirrors with smooth sidewalls (<50 nm roughness).

Progress

During FY-97 a collaboration between UCSB and LLNL was established for the development of processes necessary to fabricate GaN-based blue laser diodes. Our primary objective was to develop dry etching techniques for the fabrication of laser mirrors on GaN-based materials. Our research focus is on the quality of the dry-etched laser mirror, and not on the etch rate of the GaN. Research at UCSB focused on device design and GaN crystal growth, and provided the necessary materials for the dry etching experiments at LLNL.

As of September 1997, vertical etching of single crystal GaN was demonstrated at LLNL using CAIBE, with a Xe-ion beam and Cl_2 (**Fig. 1**).

Using existing equipment located in LLNL's MicroTechnology Center, we have evaluated CAIBE using the following gases: Cl_2, H_2, SF_6, and carbon tetrafluoride (CF_4). The etcher consists of an 8-in. ion gun from Commonwealth Scientific Corp., Alexandria, VA with a water cooled rotary stage. The reactive gases are introduced via nozzles directed at the sample.

Initial research focused on the patterning technology necessary to define the areas to be etched. This requires straight, smooth, photoresist lines and a masking material that will be resistant to corrosive ions. Due to the optically transparent nature of the GaN, techniques were developed to reduce the negative effects of internal reflections during photoresist exposure. Anti-reflective coatings of tungsten were found to be very effective in reducing internal reflections, resulting in accurate pattern replication. A bottom anti-reflective coating material from Clariant Corporation, Summerville, NJ was found to be effective as well in reducing internal reflections during photoresist exposure.

Most researchers are presently using Ni as a mask for reactive ion etching of GaN. Since nickel is very resistant to reactive gases, the patterning of Ni is typically performed by ion milling or by a photoresist lift-off process. However, the fabrication of a Ni mask with pattern definition required for the laser mirror (straight, smooth mask lines) was found to be extremely difficult under the stringent time constraints of this project. Our limited work on Ni-masking resulted in unsatisfactory line definition with rough sidewalls.

Plasma-resistant photoresist was found to be the best masking material for the laser mirror fabrication process, since it provided the best quality pattern replication with adequate resistance to the reactive gases used in this study. Etch selectivity of the GaN to the photoresist ranged from 4:1 to 2:1 for Xe beam voltages of 500 and 1000 V, respectively.

Gas mixtures of Cl and SF_6, at ratios of 10:1 and 2:1, were found to produce poor quality, rough, sloped (over-cut) sidewalls. No enhancement of etch rate or sidewall smoothness due to the addition of SF_6 to Cl_2 was observed as has been suggested.[10]

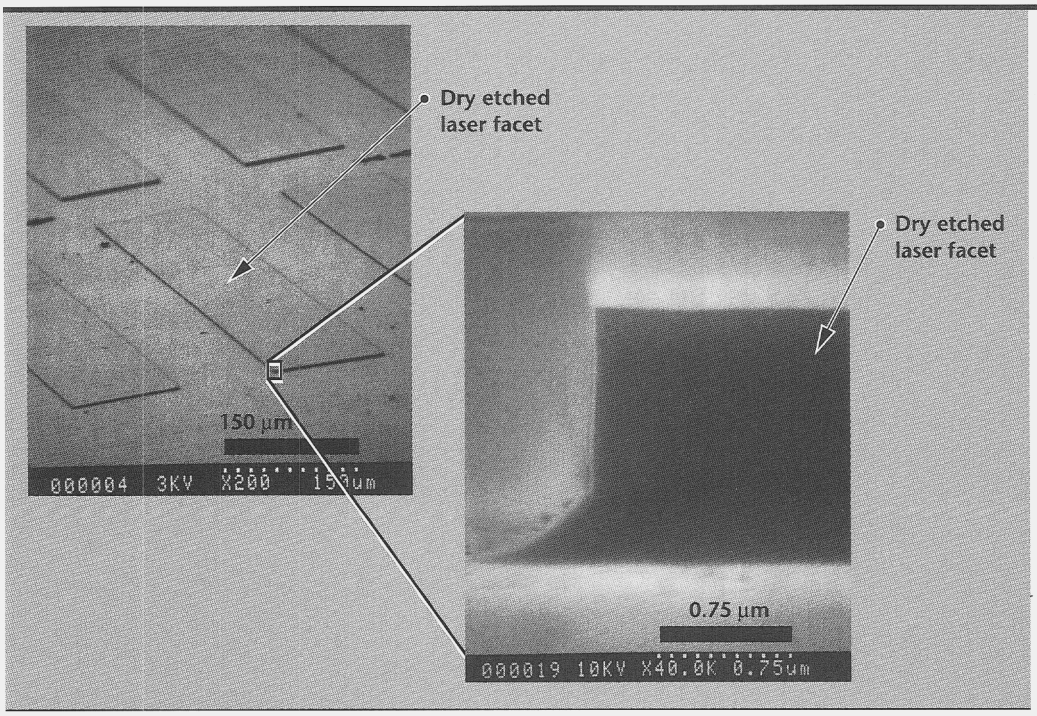


Figure 1. Scanning electron microscope (SEM) images of a GaN etched laser facet formed by chemical assisted ion beam etching (CAIBE) at the LLNL MicroTechnology Center using a 800-eV xenon ion (Xe) beam in a Chlorine (Cl_2) ambient. Note the vertical smooth sidewalls.

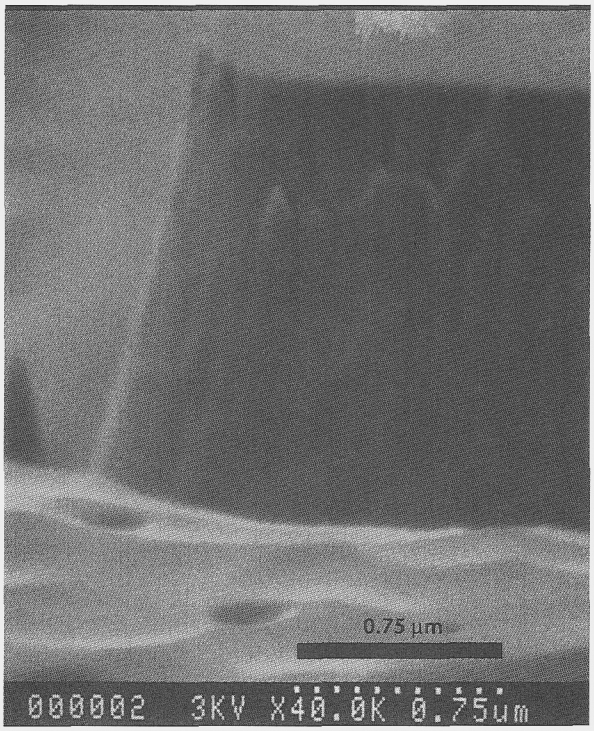


Figure 2. Scanning electron microscope (SEM) image of the corner of a GaN etched laser facet formed by chemical assisted ion beam etching (CAIBE) at the LLNL MicroTechnology Center using a 500-eV xenon ion (Xe) beam in a 10:1 chlorine (Cl_2) carbon tetrafluoride (CF_4) ambient. Note the rough morphology, sloped (over cut) sidewalls.

Cl and CF_4 gas mixtures, at ratios of 10:1 and 2:1, were found to produce rough sloped sidewalls as well (**Fig. 2**).

An enhancement in the sidewall smoothness morphology was observed, however, with the addition of 2% H to Cl. To date, our best quality vertical etching has been achieved by CAIBE using a 800-eV Xe beam in a Cl_2 ambient, achieving vertical walls with smooth sides at etch rates of 900 Å/min (**Fig. 1**). The enhanced sidewall smoothness and vertical etching was achieved by increasing the Xe beam voltage from 500 to 800 eV at beam current densities of 0.2 mA/cm^2 with a Cl_2 flow rate of 20 sccm with stage rotation. Stage rotation is useful in minimizing ion milling etch artifacts which produce sloped walls even at normal beam incidence.

Laser mirrors dry etched at LLNL on an InGaN/GaN laser device grown at UCSB recently demonstrated lasing under pulsed power at room temperatures, emitting at a wavelength of 419 nm. This demonstrates that our dry etch process developed for the fabrication of laser mirrors in GaN works. In addition, the recently developed dry etch process shown in **Fig. 1** should further enhance the efficiency of UCSB InGaN/GaN laser device.

Acknowledgments

The authors wish to thank H. Peterson, W. Goward, and S. Dijaili for technical discussions and assistance in the development of the GaN dry etching process. In addition, special thanks to M. Mack and A. Abare at UCSB for growing the GaN crystals used for the study, and congratulations to them for successfully demonstrating a blue emitting InGaN/GaN laser diode.

References

1. Kozodoy, P., A. Abare, M. Mack, K. Sink, S. Keller, U. Mishra, S. Keller, S. DenBaars, and D. Steigerwald (1997), "MOCVD growth of high output power InGaN MQW LEDs," *Materials Research Society Proceedings, San Francisco, CA,* D8.18.

2. Nakamura, S., M. Senoh, S.-I. Nagahama, N. Iwasa, T. Yamada, T. Matsushita, H. Kiyoku, and Y. Sugimoto (1996), "InGaN multi-quantum-well structure laser diodes grown on MgAl2O4 substrates," *Appl. Phys. Lett.,* **68** (15), pp. 2105–2107.

3. Nakamura, S. (1997), "III-V Nitride-based Blue/Green LEDs and LDs," *24th ISCS, San Diego, CA,* Sept.

4. Mack, M. P., A. Abare, M. Aizcorbe, P. Kozodoy, S. Keller, U. K. Mishra, L. Coldren, S. DenBaars (1997), "Characteristics of Indium-Gallium-Nitride Multiple-Quantum-Well Blue Laser Diodes Grown by MOCVD," *J. Nitride Semicond., MRS Internet,* Res. **2**, p. 41, (http://nsr.mij.mrs.org/2/41/).

5. Goward, W. D., H. E. Petersen, and S. P. Dijaili (1996), *Chemically Assisted Ion Beam Etching (CAIBE) of Precision High Quality Laser Facets on AlGaAs Quantum Well Multilayer Structures,* Lawrence Livermore National Laboratory, Livermore, CA, (UCRL-ID-124399).

6. Scherer, A., J. L. Jewell, Y. H. Lee, J. P. Harbison, and L. T. Florez (1989), "Fabrication of microlasers and microresonator optical switches," *Appl Phys. Lett.*, **55**, p. 2724.

7. Adesida, I., A. Mahajan, E. Andideh, M. Asif Khan, D. T. Olsen, and J. N. Kuznia (1993), "Reactive ion etching of gallium nitride in silicon tetrachloride plasmas," *Appl. Phys. Lett.*, **63** (20), pp. 2777–2779).

8. Ping, A. T., I. Adesida, and M. Asif Khan (1995), "Study of chemically assisted ion beam etching of GaN using HCl gas," *Appl. Phys. Lett.*, **67** (9), pp. 1250–1252).

9. Adesida, I., A. T. Ping, C. Youtsey, T. Dow, M. Asif Kahan, D. T. Olson, and J. N. Kuznia (1994), "Characteristics of chemically assisted ion beam etching of gallium nitride," *Appl. Phys. Lett.*, **65** (7), pp. 889–891).

10. Pearton, S. J., C. R. Abernathy, and F. Ren (1994), "Dry patterning of InGaN and InAlN," *Appl. Phys. Lett.*, **64** (26), pp. 3643–3645.

11. Gendron, F., L. M. Porter, C. Porte, and E. Bringuier (1995), "Hydrogen passivation of donors and acceptors in SiC," *Appl. Phys. Lett.*, **67** (9), pp. 1253–1255).

Laser Transceiver for Safeing Applications

Charles F. McConaghy
Electronics Engineering Technology Division
Electronics Engineering

Karla G. Hagans
Defense Sciences Engineering Division
Electronics Engineering

The purpose of this work has been to construct an electro-optic equivalent to a weapons safeing, arming, and detonation subsystem. The laser transceiver is a very important portion of this subsystem. An additional objective has been to evaluate the use of opto-electronics in weapons safeing applications.

Introduction

In this project, we have focused on replacing or re-inventing some of the safeing and arming functions with opto-electronics. It is believed that opto-electronics provides an extra degree of safety and security. Our design involved a fiber-based link to replace all wires and provide a high degree of electrical isolation, enhancing weapons safety. A schematic drawing of the transceiver and how it fits into the overall system is shown in **Fig. 1**.

The main functions of the transceiver are threefold. First, the transceiver receives optically modulated data via fiber and transforms it to electrical signals, which are then demodulated by electrical logic. Second, the transceiver module takes electrically-modulated data from the logic circuit and modulates it optically onto a fiber. The third function provided by the transceiver block is power generation. The electrical power to run the digital logic, as well as the transmitter and receiver, is provided by optical means. A fiber fed by a high-power laser diode is used to bring power to the transceiver. A special power converter chip converts this optical power to electrical power and acts much like a battery.

Progress

Laser Transceiver Construction

The laser transceiver is composed of elements fabricated in dissimilar technology. For example, the laser diode and power converter are both fabricated in GaAs, while the receiver chip is fabricated in Si. In addition, both GaAs parts, although fabricated in the same type of material, use substantially different processing.

These parts were fabricated by three separate commercial sources and then packaged at Lawrence Livermore National Laboratory (LLNL) into a single compact package. Although it is theoretically possible to integrate the transmitter, receiver, and power converter into one common substrate, this would have required a large research effort, and was well beyond the scope of our work. Therefore, we found it more expeditious to obtain separate, well-optimized parts from different vendors and to combine them with advanced packaging and fiber pigtailing techniques.

A large portion of the packaging is dominated by the fiber pigtails, so not much space-saving would be gained by a single integrated chip, as compared to three separate chips, as was used in this transceiver. The only difficulty with using separate parts is in identifying commercial sources willing to sell these devices in chip form.

Description of Individual Sub-Components

Both light emitting diodes (LEDs) and vertical cavity laser diodes (VCSELs) were tried for the transmitter. Although both worked, the VCSELs coupled much more efficiently to the fiber. The LEDs coupled 2 μW of optical power into the fiber for 15 mA of drive current. In contrast, the VCSELs coupled 200 μW of power into the fiber for 8 mA of drive current. The beam pattern from the VCSELs is quite circular, with a low divergence of about 8°. On the other hand, the LEDs emit light into a hemisphere, making it difficult to collect into a fiber unless a lens is used.

Horizontal fiber pigtailing was chosen to minimize package height, as well as to maximize the strain relief of the fibers. Because the fibers are horizontal, either the chips had to be mounted vertically, or some means of turning the light had to be used if the chips were mounted horizontally. The latter is the method chosen for pigtailing all three devices.

An easy method of turning the light is simply to polish the optical fibers at a 45°-angle and allow the light to bounce off the angled face. It was originally anticipated that the angled surface would have to be metalized to improve reflectivity, but almost all the light reflects off the glass/air interface, since the angle is steep enough for total reflection. The angled fiber technique was used for the fibers that pigtailed the VCSEL and the receiver chip. The only disadvantage to this approach is that the light must propagate through the cylindrical side wall of the fiber, which causes some unintentional lensing of the light.

The receiver chip is a Si device that consists of a sensor integrated with an amplifier and circuitry to generate a digital logic level output. The receiver is very sensitive and can be switched on and off with as little as 2 μW of optical power. This chip, however, does require 5V of supply voltage at a minimum of 10 mA of current drain.

The interconnection to the power source is shown in **Fig. 1**. The current drain of this chip increases proportional to the optical power that is incident on the receiver. Therefore, to minimize drain, the optical power should be only slightly above threshold.

The most unique and challenging device in the laser transceiver module is the power converter. This device acts like a constant current source with the current level set by the optical power of the incident laser light.

Power converters come in different voltage ranges achieved by variations of the series and parallel hook-ups of the array of individual cells. A 6-V device was chosen for our application since it was sufficiently high to meet the voltage requirements of both the receiver and the logic. The active area of the power converter is a 1.5-mm-diameter circle. (A 3.0-mm device was used in a later package.)

The efficiency of the power converter is 40% if the device is well heat-sinked. Current levels in excess of 100 mA at 5 V with 2 W of optical illumination were desired.

It was found experimentally that, to achieve maximum performance with these power converters, optical beam quality and positioning were critical. The maximum current is determined by the cell within the array that has the lowest optical power. Therefore, it is imperative to have all cells illuminated within the same power. One method is to use the Gaussian beam that comes out the end of a cleaved fiber. The fiber end has to be back far enough to illuminate the entire cell, but not so far back that it overfills the array. If the fiber is too close to the array, current limits may result from saturation of the power converters.

The saturation problem is handled by spreading the power over a larger area (3.0 mm, vs 1.5 mm). The 45°-fibers were found to be inadequate for giving the uniformity of illumination required by these power converters. A better method to turn the light involved the use of specially fabricated Si turning mirrors. These mirrors were anisotropically etched in Si and Au-coated. An equally effective scheme involved the use of miniature prisms attached to the end of the fiber with UV-cured epoxy. Both of these schemes gave good beam patterns on the power converters.

A 28-pin leadless chip carrier was chosen to mount all three components. This package, designed to mount electronic chips, is a .450-in.-square package that is only .060 in. tall. It is

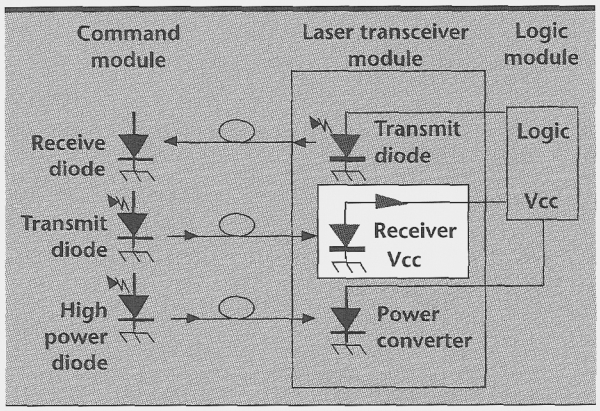


Figure 1. Laser transceiver module consisting of a transmit laser diode, receiver chip, and power converter chip.

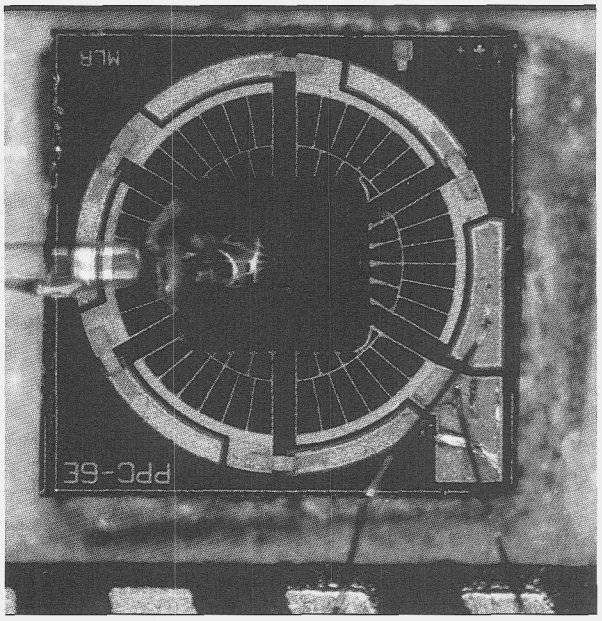


Figure 2. Power converter illuminated by fiber, with prism turning arrangement.

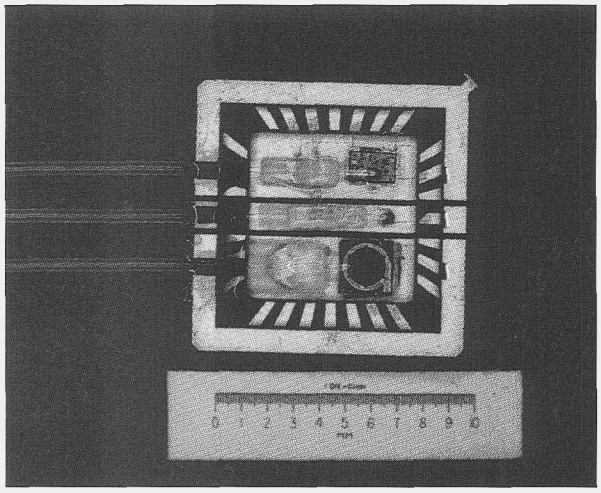


Figure 3. Completely packaged laser transceiver (less top and light shields). The receiver is at the top of the package, the VCSEL in the middle, and the power converter at the bottom. Three optical fibers exit the left side of the package.

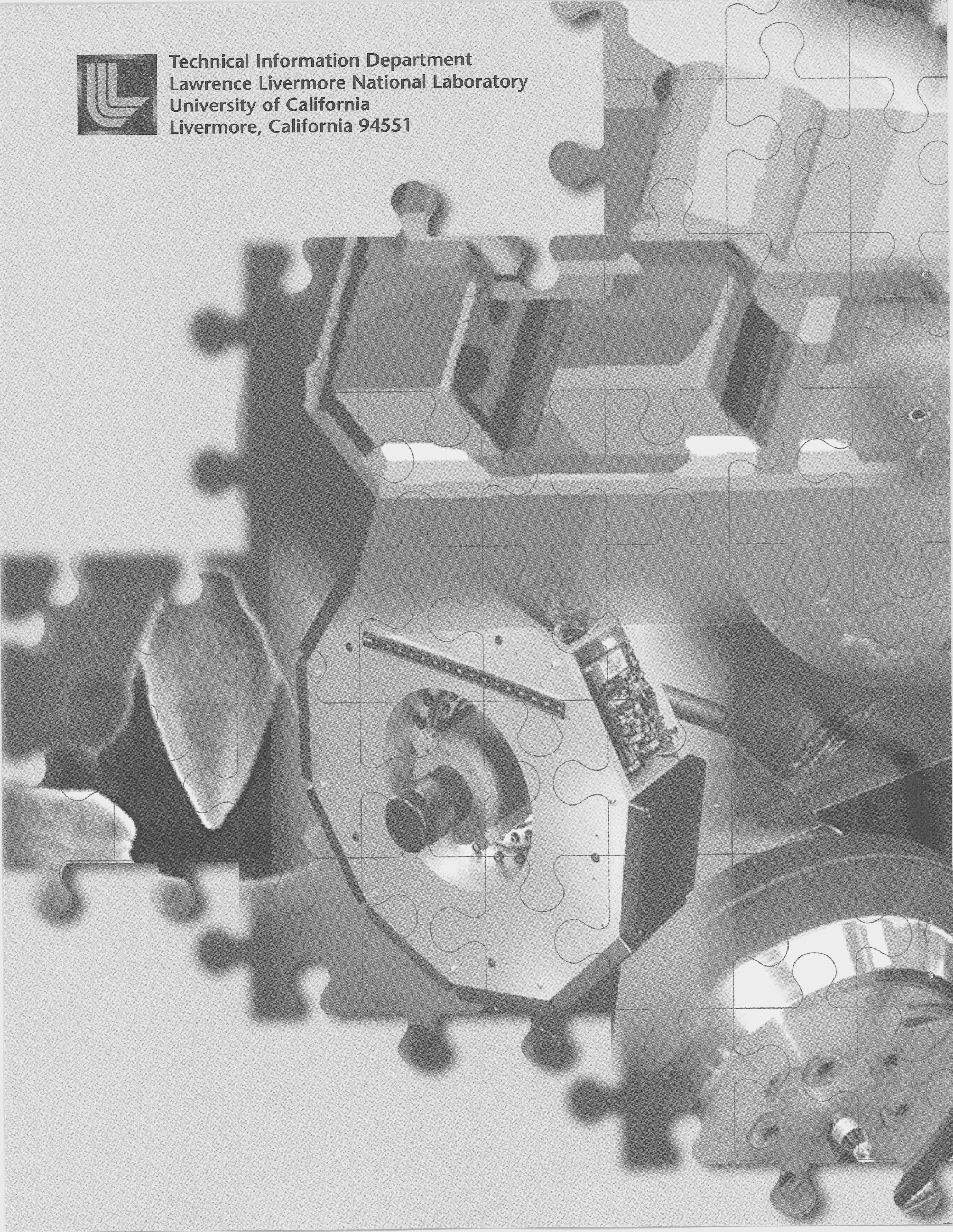
compatible with surface mounting, so it can be mounted easily on the same board as the logic. To mount optical fibers to this package, some modifications were made by precision sawing. These saw cuts allowed the fibers to protrude from the side of the package. Additional saw cuts were used to mount light shields between each of the sections of the package. **Figure 2** shows one of the power converters with a fiber pigtail attached by means of the miniature prism.

One of the main difficulties in achieving the full-current output of the power converter was getting the correct spacing between the prism and the power converter chip. For the 1.5-mm power converter, the maximum power was achieved with the prism spaced 2.5 mm away. This spacing required that the top of the package be modified to accommodate the extra space needed to illuminate the power converter. A completely packaged laser transceiver module is shown in **Fig. 3**.

Future Work

The main issue in this work was achieving the 100+ mA of current from the power converter. Future work will concentrate on new logic designs that require less current. The high-current power converters take more space, and the goal is to minimize the space of this module. Other improvements in the future would be to add optical switches to minimize the possibility of inadvertently powering the power converter.

Acknowledgments

The authors would like to thank G. Jacobson for help with all aspects of the project, from procuring parts to testing modules. We would also like to thank P. Stephan for his precision in mounting and bonding the individual components. Finally, we would like to thank R. Becker of Integrated Optical Circuit Consultants for his help in design and assembly of the modules.

Technical Information Department
Lawrence Livermore National Laboratory
University of California
Livermore, California 94551