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Nine Element Si-based Pillar Structured Thermal Neutron Detector

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ABSTRACT

Solid state thermal neutron detectors are desirable for replacing the current ^3He based technology, which has some limitations arising from stability, sensitivity to microphonics and the recent shortage of ^3He . Our approach to designing such solid state detectors is based on the combined use of high aspect ratio silicon PIN pillars surrounded by ^{10}B , the neutron converter material. To date, our highest measured detection efficiency is 20%. An efficiency of greater than 50% is expected while maintaining high gamma rejection, low power operation and fast timing for multiplicity counting for our engineered device architecture. The design of our device structure, progress towards a nine channel system and detector scaling challenges are presented.

Keywords: Thermal neutron detector, pillar, boron.

1. INTRODUCTION

The availability and fieldability issues of ^3He based thermal neutron detectors have mandated the evaluation of alternative techniques. Several different designs of solid state thermal neutron detectors are currently being investigated [1-5]. Our design is based on a high aspect ratio PIN diode pillar arrays filled with ^{10}B which we have coined the “Pillar Detector” [6-15]. In order to construct large area detection systems to replace current ^3He based systems, our approach is to assemble arrays of smaller solid state neutron detectors. This highly segmented system will be able to withstand a significantly higher neutron count rate as well as possible mapping of the location of neutron sources, compared to a single element. Moreover, the system will be lighter and smaller than ^3He tubes. Since the system is basically constructed with thin layers of neutron detector arrays, this leads to significant improvement of its portability as an inspection tool. A comparison of the primary detector figures-of-merit for our device (after appropriate scaling) and ^3He tubes is shown in Figure 1.

Thermal neutrons have a low probability of interacting with conventional semiconductor materials. Thus, a two-step detection process is generally required. First, the thermal neutrons are converted to energetic ions by a material with a high thermal neutron cross-section. In our device ^{10}B is used (its cross-section for thermal neutrons is $\sigma = 3,837$ barns) resulting in the following reaction: $n + ^{10}\text{B} \rightarrow \alpha + ^7\text{Li}$. Second, these energetic ions are then collected using a semiconductor diode. Three major criteria drive the optimal design of our thermal neutron detectors: (1) sufficient thickness of neutron converter material (50 μm thick in ^{10}B), (2) high probability of ion energy deposition within the semiconductor detector (ion track length of 3 μm in ^{10}B), and (3) large discrimination between gamma ray events and thermal neutron events. Using a three-dimensionally integrated approach, very high detection efficiency is possible because the geometrical constraints on the converter material thickness are decoupled from the limitation of the ion track length requirement [9-10], as shown in Figure 2. Here the ^{10}B thickness is defined by the pillar height (etch depth) so as to absorb the thermal neutrons. The pillar pitch is defined lithographically to allow the highest possible interaction of the energetic ions with the semiconductor pillars. Our highest efficiency of 20% to date has been achieved with an array of etched Si pillars with 13:1 aspect ratio (2 x 2 μm^2 pillars with a 26 μm etch depth or height and a separation of 2 μm) on a planar silicon substrate, arranged in a square matrix. One added benefit of this high aspect ratio is that the so-called “streaming” of neutrons becomes negligible. When the 3D pillar detector is scaled to 50 μm , a high efficiency device (>50%) is predicted [9-10]. The design of our device structure, progress towards a nine channel system and detector scaling challenges are presented.

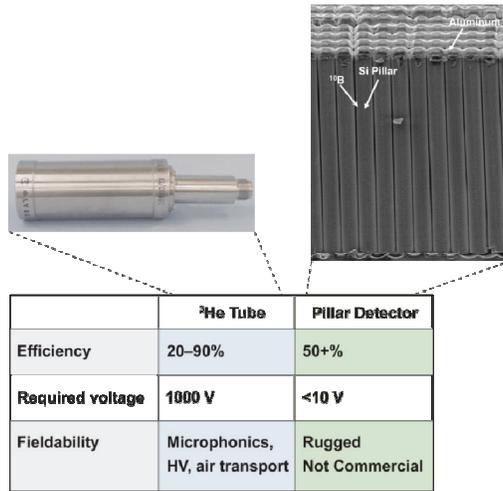


Figure 1. Comparison of the primary detector figures-of-merit for pillar structured thermal neutron detector and ^3He tubes.

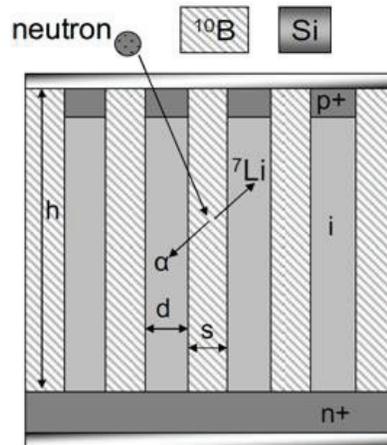


Figure 2. Schematic of a pillar structured thermal neutron detector, h: pillar height (26 μm), d: pillar size (2 μm), s: pillar separation (2 μm).

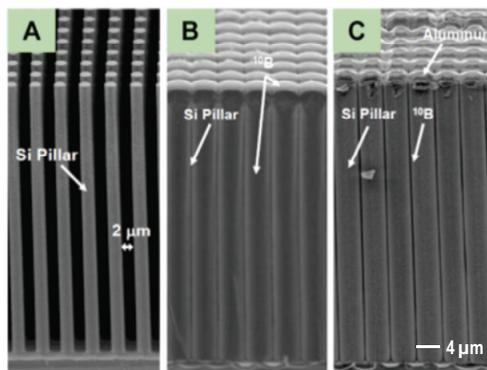


Figure 3. SEM images of 26 μm silicon pillars structures: (a) as fabricated by etching, (b) after boron deposition, and (c) after etch-back of excess boron and aluminum evaporation.

2. DEVICE FABRICATION

The fabrication process begins by epitaxially growing p+ and i layers on an n+ silicon substrate by chemical vapor deposition. The pillar diameter and spacing are then defined lithographically, followed by plasma etching to create high aspect ratio structures utilizing an SF₆ approach (Figure 3a). A conformal coating of ¹⁰B is then deposited on the pillar array by chemical vapor deposition. The ability to deposit a conformal and uniform coating of ¹⁰B [11] is one of the key steps to the success of the detector (Figure 3b). Next, the “etch-back” is carried out using a Plasmaquest electron cyclotron resonance etching (ECR) [12-13] to expose the p+ layer for uniform contact formation [14]. Lastly, after the planarization of the sample, aluminum is sputtered onto the structures to fabricate the electrodes (Figure 3c). The characterization described in the remainder of this paper (unless noted otherwise) was carried out on a detector with 2 μm diameter pillars with 2 μm spacing and 26 μm pillar height on a test chip with an area of 2 mm x 2 mm (Figure 3).

3. SINGLE DETECTOR PERFORMANCE

3.1 Electrical: current-voltage and capacitance-voltage

Current versus voltage measurement illustrates a reverse bias current density of 10⁻³ A/cm² measured at -10 V (Figure 4). Low leakage current is essential for high sensitivity to neutron events because it sets the noise floor for the device. The leakage current is comprised of bulk and surface components. The reverse biased current density of an unetched planar diode structure is on the order of 10⁻⁷ A/cm², implying that the increase in leakage current is due to surface recombination. Further reduction in leakage current for the pillar structure can be achieved by passivating the sidewalls of the pillar array which has a large surface area [15]. Low voltage is also important for low power devices. The intrinsic region of the detector has a free carrier concentration of 3×10¹³ cm⁻³, which requires -10 V for full depletion, as shown in Figure 5. The simulated electric field profile of the detector shows that the electric field becomes larger as the reverse bias increases. At low voltage, the intrinsic region is partially depleted. The reaction-induced carriers generated at the undepleted intrinsic region need to travel to the high field area by diffusion in order to be collected by the electrodes and generate a signal. The diffusion length of free carriers is related to the bulk lifetime and surface recombination velocity at pillar sidewall.

Capacitance versus voltage characteristics were measured and show a capacitance of 400 pF at 0 V and 85 pF at -10 V, as shown in Figure 6. The measured voltage integrated over the shaping time for the detector is inversely proportional to the capacitance. Therefore, it is important to minimize the capacitance. Increasing the intrinsic region thickness or applying a reverse bias can effectively decrease the capacitance of the device. However, this in turn will result in the increase in leakage current. The optimal depleted intrinsic region thickness as well as the bias point needs to be optimized to maximize the neutron detection efficiency.

3.2 Gamma rejection

The discrimination between gamma ray events and thermal neutron events was measured by exposing the detector to 662 keV gamma rays from a 10 μCi ¹³⁷Cs source, yielding 6 gamma ray counts during the 12 hour measurement. The very low gamma response indicates a neutron-to-gamma discrimination ratio of ~ 10⁵. We attribute the low gamma detection efficiency to the low linear attenuation coefficient (μ), and exceedingly short thickness of the active region, which accounts for the probability of interaction. For the energies of interest, 100 keV to 2 MeV the gamma interaction cross-section is dominated by Compton Scattering [16] and therefore the μ can be readily determined. For the upper bound gamma energy of interest, γ = 2 MeV gives a μ = 0.10 cm⁻¹ [16], which is dependent on the low atomic number Z = 14 and density ρ = 2.33 g/cm³ for Si. The low μ, in addition to the pillar height (26 μm), is responsible for the low number of gamma counts being registered and correspondingly large neutron to gamma discrimination.

For comparison with measurements, the gamma detection efficiency was simulated using MCNP [17] for a 5mm x 5mm area array of 2μm x 2μm Si pillars of various heights using a point gamma source of varying energies, where gamma efficiency is defined as the number of simulated gamma interactions that result in an energy deposition of greater than 50 keV divided by the number of incident gammas. The gamma detection efficiency as a function of pillar height for two different gamma energies (662 keV and 1.3 MeV) is shown in Figure 7. As the pillar height is increased, the gamma efficiency is also increased. Also as the gamma energy is decreased the gamma detection efficiency increases due to the higher probability of the gamma interaction with the Si pillar array. The simulated gamma discrimination is found by

dividing the simulated neutron detection efficiency by the simulated gamma detection efficiency. Also shown in Figure 7 is the simulated gamma discrimination as a function of pillar height for two different gamma energies 662 keV and 1.3 MeV. The gamma discrimination is relatively constant versus pillar height because the gamma detection efficiency and neutron detection efficiency have similar pillar height dependencies over the range of simulated pillar heights.

Other semiconductor based thermal neutron detectors have been reported to have neutron to gamma discrimination ratios of 3×10^6 for ^{60}Co [18]. These values can be compared to ^3He tubes which have very low intrinsic gamma detection efficiencies of 1×10^{-9} and thus neutron to gamma discrimination ratios on the order of 10^8 .

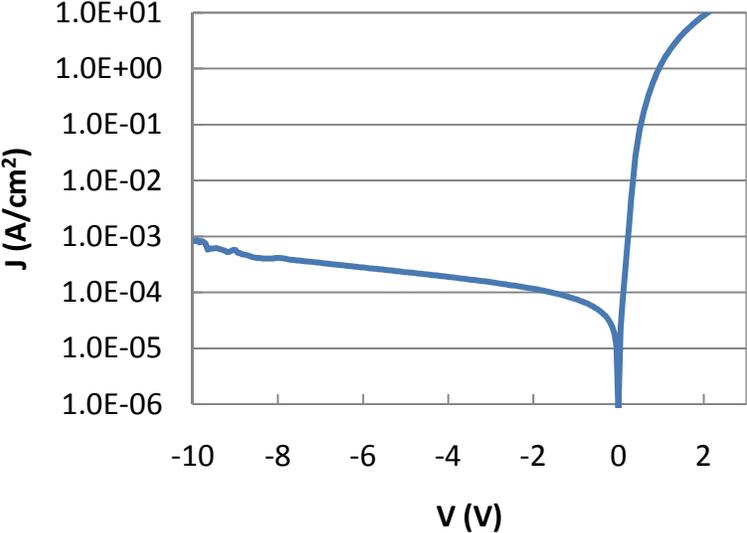


Figure 4. Measured current-voltage characteristics.

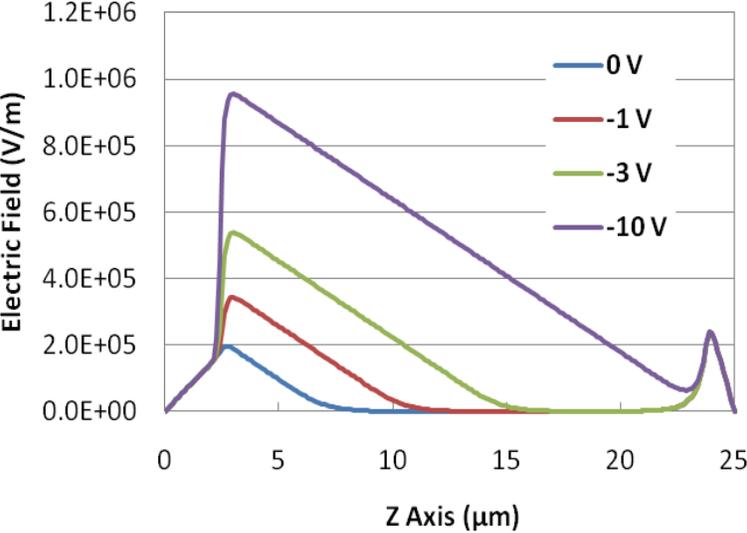


Figure 5. Calculated electric field of a single detector at varied reverse biases.

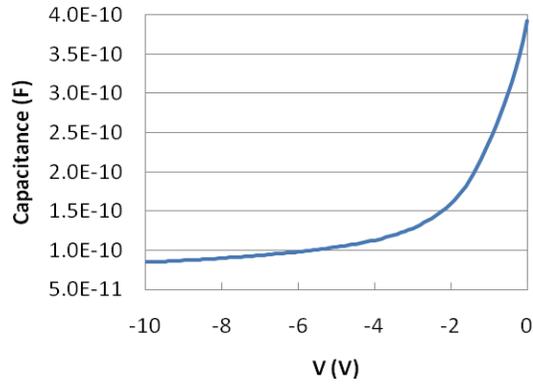


Figure 6. Measured capacitance-voltage characteristics.

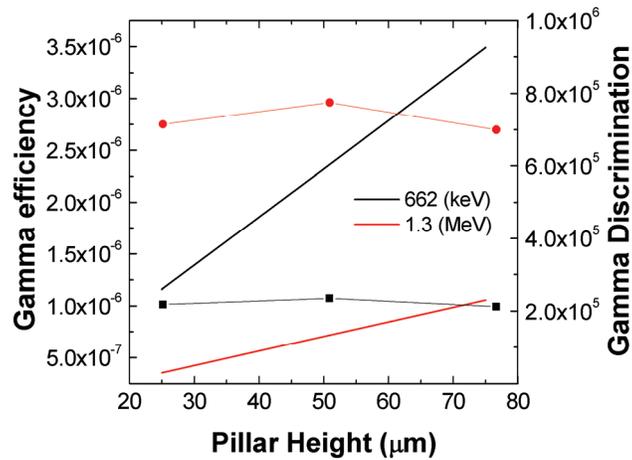


Figure 7. Calculated gamma detection efficiency (lines) and gamma discrimination (symbols) of $2\mu\text{m} \times 2\mu\text{m}$ pillar array versus pillar height for gamma-ray energies of 662 keV and 1.3 MeV.

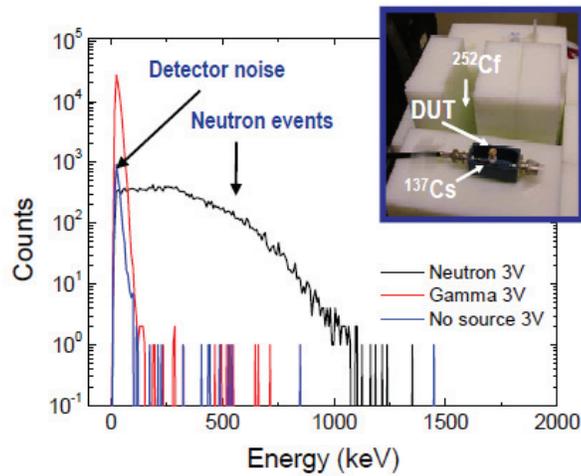


Figure 8. Measured neutron detection spectrum and gamma detection spectrum of the pillar structured thermal neutron detector with $26\mu\text{m}$ silicon pillars structures. The inset shows the test configuration.

3.3 Neutron response

The neutron response was measured using a ^{252}Cf fission neutron source with intensity of 2×10^6 neutrons/sec and moderated by polyethylene blocks of ~ 6 -inch thickness to yield thermal neutrons. For this experiment, the measurement time was 12 hours, where a 0.5 micro-second shaping time was used and the energy is calibrated with $^{243}\text{-}^{244}\text{Cm}$ source which has an alpha energy peak of 5.5 MeV. Because the neutron source strength decays over time the calibration structure was re-measured to determine the current thermal neutron source strength using the known standard efficiency of 7.3% [9]. Using this source strength and the measured neutron counts/min efficiency is determined. Specifically, the detection efficiency is determined by integrating all counts above the noise level of 110 keV which gives a thermal neutron detection efficiency of 20 % at -3 V.

4. DEVICE SCALING

To date, thermal neutron efficiencies of 3.5, 7 and 20% have been benchmarked for pillar heights of 6, 12 and 26 μm tall. Taking into account leakage current through the device which sets the low level discriminator, it is estimated that an efficiency of 50 % can be achieved with a pillar height of about 50 microns. Devices are currently being processed to meet this target.

Besides scaling for efficiency, work is also being done to scale the wafer process piece size and detector element size. Wafers are currently being processed that are two inches in diameter. All process steps are compatible with batch wafer processing and are therefore fully compatible with conventional 4 inch silicon wafer lines or larger.

In terms of maximum element size, the leakage current and capacitance play a role. When evaluating the detector efficiency the applied voltage has been swept from zero to ten volts and the efficiency changes an insignificant amount. This is interesting from a device physics point of view as the intrinsic region is not fully depleted when the device is at a zero or low voltage setting, this can be seen in Figure 5. This illustrates that the charged carrier diffusion length in the silicon pillar array is adequate to fully collect the charges generated by the neutron flux. Even if the detector is unbiased a current will be developed when the sensed charges are being collected, therefore, having a low leakage diode is still important. As can be seen in Figure 6 at 0V the capacitance is 400 pF and reduces to 150 pF at -2V. Clearly there is a tradeoff in setting the bias voltage in terms of noise within the detector from either high capacitance or high leakage current. The neutron counts are reduced for a detector with larger noise as the neutron counts will be lost within the large signal generated from noise. The point at which the generated counts equal the counts from noise is where the low level discriminator is set. Additional work needs to be done in order to determine the optimal bias point.

5. PERFORMANCE OF 9-ELEMENT DETECTOR

The performance of the 9 element detector was done by measuring both the current-voltage characteristics and thermal neutron response; this is shown in Figure 9. The neutron measurement was done using a ^{252}Cf source moderated by placing the source within a Cd coated D_2O water filled moderating sphere. The source was placed 1.5 m from the detector. The detectors were measured at 0 V for 3000 s. Integrating the total counts above the background yields 14 counts/sec/cm².

6. DESIGN OF READ-OUT ELECTRONICS

The readout electronics is a custom design based on a well-known topology [19]. The design described in [19] was originally developed to provide Germanium-quality performance. In this case, such a level of performance is not required and several compromises could be made to optimize the design for low power while preserving adequate bandwidth (20 ns risetime). The fast response is needed in order to provide adequate timing for coincidence measurements. The noise profile of the system is different than most standard applications, in that the dominant noise in the readout is given by the detector leakage current. Therefore, the input JFET was not chosen, as in common practice, to capacitively match the detector, but to give negligible overall noise contributions ($1/f$, white and current noise) to the overall noise figure for the lowest reasonable current consumption ($\sim 1\text{mA}$ drain current). For sake of simplicity, and to allow the capability of collecting holes or electron signals, the power supply rails have been kept at $\pm 12\text{V}$, as in the original design, but further optimization on their value could be done to further lower the power consumption.

The preamplifier is followed by a fast shaper using a semigaussian, fourth order bipolar shape with 250ns peaking time. The reason for this choice was to minimize the dominant noise component, the detector's current noise associated with its leakage current. Bipolar shaping poses a penalty to the white (high-frequency) noise components but is more tolerant to the lower frequency components [19] and offers intrinsically better baseline return than unipolar signals, mitigating the need for a baseline restoration circuit. In fact, given the expected neutron rate and the previous argument, the use of a baseline restorer was deemed not necessary at this stage of the design. The shaper optimizes the signal-to-noise ratio for the signal and its output is fed to a simple low power, leading edge comparator that detects the presence of a signal, but the shaper output is also capable of driving 50 ohm loads for different applications.

Additional logic gates combine the event detection signals from any of the 9 channels to give an overall detection rate response or a detection rate per-channel. Multiplicity counting can also be easily implemented by external logic. In order to give simple visual feedback, the logic includes a 3x3 LED matrix that signals on a channel-by-channel basis the presence of events.

A large amount of flexibility for testing was given, by implementing, at the layout level, several options for detector footprint. Up to four standard TO-type metal cans with single detectors can be used with or in lieu of an array of bare detectors arranged on a daughter board (referred to as 'interposer card'). Once populated with detector dies, an interposer card can be connected to the 9 channel readout system via a low profile connector. Particular care was given in the circuit layout to minimize strays. Figure 10 shows a picture of a 3 x 3 array of detectors integrated into the 9 channel readout system.

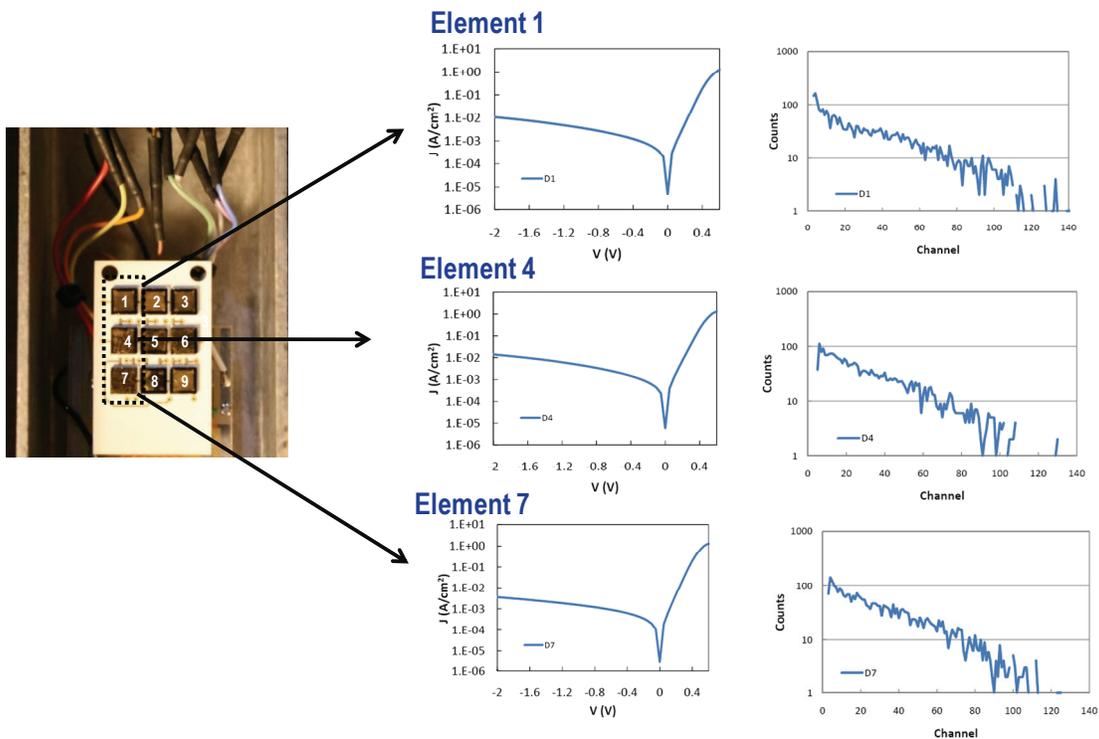


Figure 9. Nine element detector. Each detector has an active area of 2 mm x 2 mm. Current vs. voltage and thermal neutron response are shown for the first column of the 3 x 3 set.

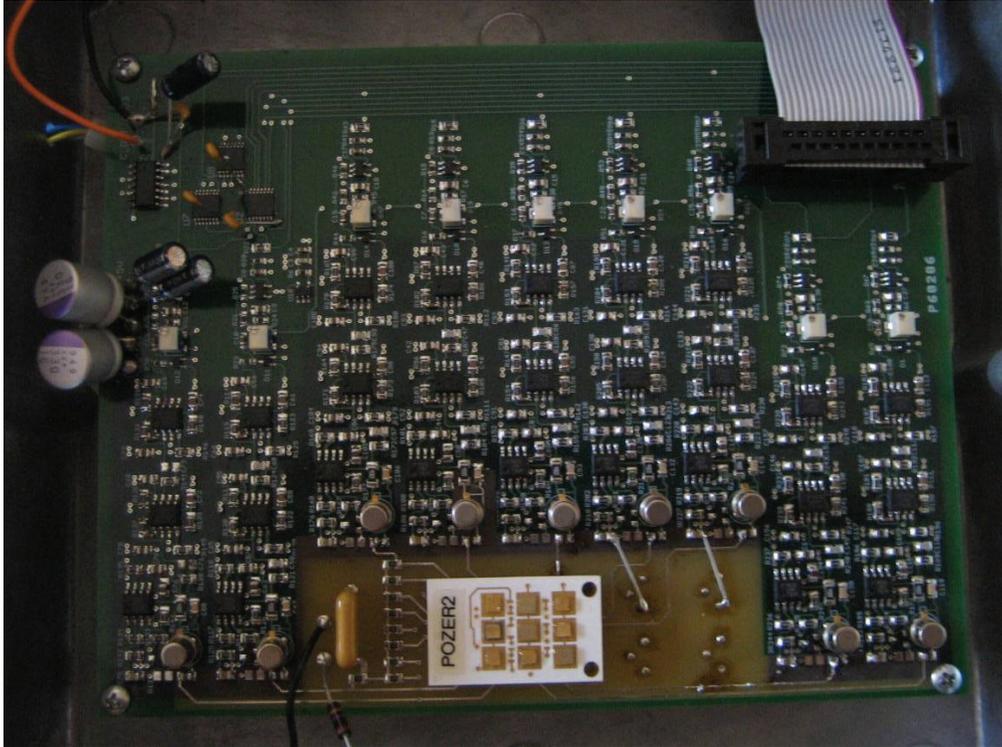


Figure 10. Nine channel COTS readout integrated with nine element pillar detector array.

7. CONCLUSION

We have shown that semiconductor based neutron detectors can be a ^3He replacement. Silicon is an ideal material system for electron/hole collection and ^{10}B is an ideal neutron conversion material due to its high thermal neutron cross-section and compatibility with silicon foundry processing. High aspect ratio structures of $2\ \mu\text{m} \times 2\ \mu\text{m}$ pillars, with a $4\ \mu\text{m}$ pitch achieves a 20 % thermal neutron detection efficiency with neutron to gamma rejection of 10^5 owing to the exceedingly short active region thickness. The design, fabrication and characterization of a 3×3 array of $2\ \text{mm} \times 2\ \text{mm}$ elements to build up a total area of $6\ \text{mm} \times 6\ \text{mm}$ shows a thermal neutron count rate of $14\text{n}/\text{sec}/\text{cm}^2$ for a moderated ^{252}Cf source 1.5 m from the detector. We have designed and built a COTS read-out circuitry for our 9 element detector. Additional work is needed to integrate our 9 element detector with the COTS readout.

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