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HPCS PRODUCTIVITY STUDY – COMPILER ANALYSIS SUMMARY

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Table of Contents

Table of Contents 3
Compiler Analysis Summary 4
Appendix 6
Compiler Statement of Work - HPCS Phase III Productivity Activity: Productivity Evaluation 6
Compiler Evaluation 6
Background 6
Statement of Work: 6
Tasks, Milestones, Deliverables, Schedules: 6
Telecons Between IBM, DARPA, ORNL, and LLNL 7
Telecon Meeting September 16, 2010 7
Telecon Meeting October 28, 2010 8
Telecon Meeting November 24, 2010 9
Telecon Meeting December 15, 2010 9
Telecon Meeting February 17, 2011 9
Telecon Meeting April 14, 2011 9
Results of Tests Run by Bor Chan, LLNL 11

Compiler Analysis Summary

As part of the HPCS Phase III Productivity Activity: Productivity Evaluation (D12683), Lawrence Livermore National Laboratory (LLNL) evaluated the IBM *PERCS* compliers, focusing on IBM's POWER 7 chip. The goal of this analysis was to evaluate the *PERCS* compilers (C and FORTRAN) coupled to the POWER 7 chip under various scenarios using established benchmarks that Bor Chan, a Computer Scientist from LLNL, had expertise using on multiple platforms.

The Benchmark Codes used were

Benchmark	Explanation
Crystal	Single CPU optimization and SIMD compiler challenge.
IRS	**Marquee performance code**. Single physics package code. Implicit Radiation Solver for diffusion equation on a block structured mesh.
UMT	**Marquee performance code**. Single physics package code. Unstructured-Mesh deterministic radiation Transport.
CAM	Kernels from an atmospheric benchmark suite
MF24	Livermore Loops; 24 do-loops; Each loop carries out a different mathematical kernel
EPCC	OpenMP benchmark to evaluate the overhead of OpenMP

Eight tests were run with these benchmark codes comparing the POWER7 (P7) chip to both the POWER5 (P5) chip and the BlueGene (BG) architectures.

Test Name	What was tested	Summary of Results
P5_P7	OpenMP Overhead	For two threads, generally P7 showed good speedup, however for 4 and 8 threads, P7 had poor performance
P5_P7.CRYSTAL	Effectiveness of MASSV on P7	Overall, P7 showed good speedup.
P5_P7.IRS	Effectiveness of the 12 prefetch streams that P7 has	Overall, P7 showed good speedup
P5_P7.UMT	• How well the compiler can unroll the loop • Generate SIMD instruction *without* actually vectorizing the loops • Compare C and FORTRAN	• Overall, P7 showed good speedup. • Note that this benchmark has been tuned for BG machines, and the vector units on those platforms, and even so, with different chips and the associated different overheads, the P7 did well. • The P7 without the SIMD speedup was greater than the clock speedup which is extremely good. That implies the compiler is doing a great job especially in C. • The unroll did not enhance SIMD as BGQ does.
P7_BG.CAM	Test loop	Some of the tests showed better performance on P7 versus

	optimization	BG machine, while some tests had slightly worse performance. No large discrepancies were noticed.
P7_BG.MF24	• SIMDzation on P7 • Compare C and FORTRAN	Some of the tests showed better performance on P7 versus BG machine, while some tests had slightly worse performance. No large discrepancies were noticed.
P5_P7.epcc	Evaluate the overhead of the P7 with OpenMP	• Most of the timing improvements for P7 is for 2 threads. • Comparing with P5, 2/4/8 threads shows significant slow down for SINGLE, CRITICAL, LOCK/UNLOCK an ATOMIC. (except 2 threads timing for SINGLE) • Among various P7 versions of compiler, the latest version is slightly better.
P5_p7.matrix	Effectiveness of various hardware matrix performances	• Hardware matrix performance tests using UMT • P7 is the first compiler to deliver better wall time speedup compare with clock rate speedup of the chip. That translates to excellent compiler work. • Significantly fewer instructions for P7 – half – and 2/3 cycles compared to P5

All parties to this endeavor agree that the evaluation met the original goal stated above. The collaboration proved fruitful in uncovering some shortcomings to the PERSC compiler and in showing its strengths, as stated in the results above. The monthly telecons between the invested parties were instrumental in keeping the project on-task, and in relaying information to IBM in a timely manner.

Appendix

Compiler Statement of Work - HPCS Phase III Productivity Activity: Productivity Evaluation

Compiler Evaluation

Background

This statement of work is to clarify expectations for a compiler evaluation that is part of the HPCS Phase III productivity evaluation outlined in a WFO Proposal between LLNL, ORNL and DARPA. Discussions have occurred between IBM/Toronto's Yaoquing Gao, XL compiler technical lead for PERCS project, and LLNL Bor Chan to narrow the scope of work and understand the features available with the POWER7 FORTRAN/C/C++ compilers.

This PERCS compiler collaboration work will not be tied to any DARPA milestones. Through this effort, PERCS mission partners can benefit from knowing more about how to do performance tuning on POWER7 using IBM XL compilers, and IBM compiler side can benefit from the feedback from PERCS mission partners on compiler performance and productivity enhancement for future consideration.

Statement of Work:

LLNL Plans to evaluate the following complier features:

1. SIMDzation on POWER7.
2. The effectiveness of MASSV on POWER7.
3. Various compiler optimization flags for code transformations.
4. The effectiveness of the 12 prefetch streams that P7 has.
5. Compare performance between C and Fortran compiler for the same code.

Tasks, Milestones, Deliverables, Schedules:

1. We will use Power5 timing as a base line as long as we have the machine in site.
2. We will use MF24 to test item 1.
3. We will use Crystal to test item 2.
4. All benchmarks will use various compilation flags for item 3.
5. We will use IRS to test item 4.
6. We will use UMT/MF24 to test item 5.
7. We will use UMT to test how well the compiler can unroll the loop and generate SIMD instruction *without* actually vectorize the loop.
8. We will use a optimize UMT kernel used in BG/Q test to compare its performance against Power7.

9. As each part is completed, we will report our findings in a technical report. All sections will be complete by April 30, 2011.

Telecons Between IBM, DARPA, ORNL, and LLNL

Telecon Meeting September 16, 2010

Agenda:

1. Round-table introduction;
2. Discuss compiler collaboration with PERCS mission partners:
   - Requirements
   - Expectations for collaboration
     - Provide compiler information to DARPA mission partners: new compiler features to exploit Power7 hardware, options, directives for performance tuning
     - Gather information from DARPA mission partners on benchmark and application code analysis, from possibly manually tuning critical code to compiler auto optimizations;
     - Get feedbacks and address new requirements from DARPA mission partners on compiler performance and productivity for future enhancement
   - How often we gather together, etc.
   - Other items?

Attendees:

PERCS mission partners:

Jeffrey Vetter (ORNL)

Bor Chan (LLNL)

IBM:

Yaoqing Gao (XL compiler technical lead for PERCS project),
Robin Green (XL compiler manager for PERCS project)
Ettore Tiotto (XL UPC compiler technical lead for PERCS project)
Patricia Clark (PERCS project manager)
John Richards, Catalina Danis, Cal Swart (Productivity assessment team)

Discussion:

The initial scope for this compiler collaboration is for C/C++/Fortran. We can discuss extending the scope later if needed.

Jeffrey mentioned that Dolores had been fostering the collaboration. She had ideas about getting compilers in hands of users. Jeffrey also mentioned that Yaoqing Gao had given a nice presentation on some new compiler features at one of the MS meetings and he is interested in getting it out to folks using it. Jeffrey suggested gathering some information from DoD folks.

Bor Chan would like to know:

- How the P7 vector unit works, to help Bor understand BG/Q vs P7 behavior of microkernels.

- Compiler Intrinsics
- ESSL and parallel (vector) ESSL
- MASS and MASSV
- New Compiler optimizations (polyhedral, advanced memory, assist threads, XML transformation reports) and other compiler optimizations we added for POWER7 in V11/V13
- POWER 7 Architecture and hardware information and impact of hand-tuning for one architecture on getting good performance on another : Bandwidth, L1/L2/L3 cache characteristics, set associativety , SMT, the overhead to start a thread on POWER5 vs POWER7. SIMDization/short vectorization, long vectorization. prefetch, etc.
- Bor knows the UMT benchmark fairly well (Sequoia benchmark) and would like to see how poly and other optimizations affect performance of that benchmark.

From IBM compiler side,

- We can provide some documents and tutorials in the collaboration meetings to help the mission partners to get familiar with XL compilers and POWER7 hardware features. We just shipped XL C/C++ V11.1 and XL Fortran V13.1 on both AIX and LINUX for POWER7. We will provide the information on what features are new, and on how to use new compiler features to exploit POWER7 hardware.
- We would like to gather information on what application performance challenges PERCS mission partners are facing, and what kernels and benchmarks /applications they are interested in. We would like the mission partners can work with us to conduct code analysis to identify performance opportunities and requirements for future compiler enhancements.
- To improve the productivity, the latest IBM XL compiler release supports compiler transformation reports in XML. Users can view an XML report using a browser, or navigate it using a new tool prototype called Compiler Feedback View in the PTP tool. Users can also use tools such as HPCS toolkit for compiler transformation reports. We would like to get feedbacks on how the compiler transformation reports can help them do application performance tuning, and any new enhancement they would like to see.

Action items:

1. PERCS mission partners: Get access to POWER 7 system. Dolores should be working on getting Bor on M166. Jeffrey will send Joe Cross a message and cc Bor.
2. Bor also suggested Jeff/Evi…etc should start working on SOW (Statement of work) for LLNL.
3. IBM will provide documents on IBM compilers and MS compiler presentations to help bring Bor and DOD folks up to speed on compiler optimization so far.
4. There was no DoD representation in today's meeting due to a meeting conflict. Jeffrey suggested that we gather some feedback from them.

Telecon Meeting October 28, 2010

Agenda:

1. PERCS compiler collaboration SOW discussion (all);
2. Performance tuning tips on POWER7 using IBM XL compilers (Yaoqing Gao/IBM);
3. Initial kernel analysis and tuning (Bor Chan/LLNL)

Action items:

1. provide POWER7 hardware information and performance counter information (to be done)
2. provide OpenMP environment variable setting for Bor to tune OpenMP code (done)
3. provide PERCS mission partners the compiler presentation schedule in SC10 (to be finalized)
4. Bor will provide the source of UMT (done), XL compiler team will investigate O3 vs. O5 performance and discuss it in the next meeting;
5. Provide PERCS mission partners with the presentation slides of performance tuning on POWER7 using XL C/C++/Fortran compilers (done, the draft slides sent to Dolores)
6. Schedule the next meeting in the week of before or after SC10 (to be finalized)

Telecon Meeting November 24, 2010

Agenda:

1. brief review of the list of action items and open discussion on compiler collaboration (performance and productivity)
2. benchmark measurement and analysis update (by Bor) *(See attached file: p5_p7.CRSTAL)(See attached file: p5_p7.IRS)(See attached file: p5_p7.UMT)*
3. compiler optimization investigation update (by IBM) *(See attached file: umtmk.ppt)* by Tommy *(See attached file: IRS performance analysis.ppt)* by Salem

Telecon Meeting December 15, 2010

Agenda:

1. Review of the list of action items from the previous meetings;
2. Summary of productivity discussion from Catalina
3. Benchmark analysis update from Bor *(See attached file: P7_BG.CAM) (See attached file: P7_BG.MF24)*
4. Compiler optimization investigation update from IBM *(See attached file: CrystalMk performance analysis.ppt) (See attached file: irs_crystal.ppt)*

Telecon Meeting February 17, 2011

Agenda:

1. PERCS compiler collaboration update
2. Benchmark analysis update from Bor *(See attached file: P5_p7.epcc)*
3. PERCS compiler technology deep dive session --- Polyhedral framework by Salem *(See attached file: Polyhedral from user's perspective.ppt)*
4. Upcoming activities

Telecon Meeting April 14, 2011

Agenda:

1. Analysis update by Bor;[attachment "p5_p7.matrix" deleted by Yaoqing Gao/Toronto/IBM]
2. Follow-up PERCS compiler technology deep dive session -- Advanced Memory Hierarchy Optimizations, XML compiler transformation reports[attachment "Advanced memory hierachy optimizations from user's perspective.ppt" deleted by Yaoqing Gao/Toronto/IBM]
3. Technical discussion and actions

Attendances:

Dolores Shaffer
Bor Chan (LLNL)
Evi Dube (LLNL)
Patrica Clark (IBM)
Yaoqing Gao(IBM)
Shimin Cui (IBM)
Wang Chen (IBM)

Summary:

1. Bor presented performance analysis from hardware aspect with the following summary:

- The project finished on time and within budget. We deliver more than we promised (OMP overhead analysis and detail analysis of the code generated by the compiler for UMT).
- For the power series chips, P7 is the first compiler deliver better wall time speedup compare with clock rate speedup of the chip. That means excellent compiler work.
- Many thanks to IBM's compiler group. It provides in depth information for the new compiler technologies and how to take advantage of them.

Result of UMT:

- Wall time speedup better than the clock rate speedup.
- Compiler generates only half of the instructions and use 2/3 of cycles compare with P5.
- The cache miss is about the same as P5 but DTLB miss is much less.
- Branch mispredict-take/not taken is better in P7 compare with P5.
- Various units stall less on P7 except for stall caused by D cache miss.

2. The compiler collocation has been very productive. Many thanks to Dolores and Evi to promote and support the compiler collaboration, to Pat and Vickie to support this project. In particular, many thanks to Bor for the great job he did. So far, we have covered all line items in SOW. The analysis and feedback will help compiler performance and productivity enhancement. In this project, IBM compiler side arranged a series of compiler technology deep drive sessions.
3. Shimin from IBM compiler side presented Advanced Memory Hierarchy Optimizations

Action items:

1. Evi and Dolores are going to get together to discuss collaboration;
2. IBM compiler side will review the analysis work done by Bor.

Results of Tests Run by Bor Chan, LLNL

P5_P7									
	Date : 10/2010								
	Base line:								
	Running on pdev(power5)								
	Compilation line:								
	CFLAGS = -c -O3 -qhot -qalias=allp -qarch=auto -qtune=auto -qcache=auto -qsmp=omp -qlanglvl=extc99								
	LDFLAGS = -blpdata -qsmp=omp								
	//***** P7 3.36GHz 1.77XP5								
	same as above								
	All timings are in microseconds								
	Timing are for *overhead*								
		2ths		4ths		8ths			
		P5	**P7**	**P5**	**P7**	**P5**	**P7**		
	PARALLEL	1.90166	1.219966	3.248097	68.238533	1.06520E+01	244.7267		
	FOR	2.518771	1.019945	3.527094	25.629115	5.47109E+00	190.9917		
	// much higher S.D.								
	PARALLEL FOR	2.401159	1.41845	3.849722	57.871151	5.58812E+00	231.0419		
	BARRIER	0.769088	0.52798	1.00515	28.419244	1.46213E+00	206.5464		
	SINGLE	0.271568	0.554278	0.33492	19.5683	7.41677E-01	210.7851		
	CRITICAL	0.283421	0.077162	0.346874	0.145243	3.66574E-01	0.161087		
	LOCK/UNLOCK	0.167	0.073	0.2000	0.1329	2.2019	0.1331		

		524	493	47	62	7E-01	19		
	ORDERED	0.399146	0.307467	0.452043	4.905069	5.35135E-01	124.5255		
	ATOMIC	0.117996	0.078062	0.260021	0.095265	3.99907E-01	0.072527		
	REDUCTION	2.132506	1.26574	3.569279	32.602822	5.38495E+00	248.4178		
	Note:								
	1) 2 ths have good speedup vs P5n except SINGEL								
	2) Others show *horrible* overhead except CRITICAL/LOCK/ATOMIC.								
	Assumed clock rate								
	1900 MHz 3360 MHz		2ths		4ths		8ths		
			P5	**P7**	**P5**	**P7**	**P5**	**P7**	
	STATIC		2.051294	1.878345	3.361821	4.78063E+01	7.135952	217.003	
	STATIC	1	18.915832	5.550802	32.178211	7.74538E+01	48.78656	244.6693	
	STATIC	2	9.740627	4.229712	15.6636	6.89358E+01	25.21364	225.0537	
	STATIC	4	5.888569	3.033984	7.756495	5.34789E+01	13.03698	201.1117	
	STATIC	8	3.793812	2.391291	5.275893	4.73920E+01	7.722831	198.8135	
	STATIC	16	2.809644	2.090931	4.129624	5.09230E+01	6.527126	222.976	
	STATIC	32	2.348399	1.939476	3.605783	4.04043E+01	6.115985	206.4996	
	STATIC	64	2.119505	1.857185	3.589332	5.34951E+01	5.815911	192.6477	

	STATIC	128	2.073944	1.814353	3.416967	4.97069E+01	5.668497	210.5584	
	DYNAMI	C 1	64.798427	13.424659	153.201056	9.35220E+01	452.1082	359.5859	
	DYNAMI	C 2	29.188836	7.380307	76.419139	5.81090E+01	228.2417	230.5835	
	DYNAMI	C 4	14.425886	4.669988	46.847069	6.61361E+01	131.6797	168.3821	
	DYNAMI	C 8	5.480707	3.169262	22.460532	4.56549E+01	72.0499	172.8444	
	DYNAMI	C 16	3.054917	2.399695	7.538629	4.95283E+01	33.94806	156.7164	
	DYNAMI	C 32	2.038908	1.989937	3.317833	4.41750E+01	12.78335	152.906	
	DYNAMI	C 64	1.482737	1.773524	2.858698	3.97130E+01	5.3635	153.7034	
	DYNAMI	C 128	1.268578	1.664484	2.893615	3.14725E+01	5.170882	167.339	
	GUIDED	1	4.87628	2.972913	12.822092	4.67971E+01	41.13542	167.9269	
	GUIDED	2	3.364742	2.541709	9.750092	4.78373E+01	31.31335	164.7702	
	GUIDED	4	2.615678	2.199817	8.405089	3.89539E+01	25.65813	169.717	
	GUIDED	8	1.757371	2.292144	6.638587	4.59571E+01	22.79103	160.8768	
	GUIDED	16	1.692593	2.377093	4.682589	4.72942E+01	16.17611	144.567	
	GUIDED	32	1.549172	2.26537	3.237963	4.63746E+01			

	GUIDED	64	1.430082	1.813042					
	Note:								
	1) 2ths general show good speedup except DYNAMIC 64+ and GUIDED 8+								
	2) 4ths show *horrible* result for STATIC DYNAMIC 4+ and								
P5_P7.CRSTAL									
	Date : 10/2010								
	Base line:								
	Running on pdev(power5)								
	Compilation line:								
	// O3								
	CFLAGS = -c -O3 -qhot -qalias=allp -qarch=auto -qtune=auto -qcache=auto -qsmp=omp -qlanglvl=stdc99								
	LDFLAGS = -blpdata -lmassv -lm -qsmp=omp								
	// O5								
	replace -O3 with -O5								
	//***** P7 3.36GHz 1.77XP5								
	// O3								
	CFLAGS = -c -O3 -qhot -qsimd=auto -qhot=novector -qalias=allp -qarch=auto -qtune=auto -qcache=auto -qsmp=omp -qlanglvl=stdc99								
	LDFLAGS = -blpdata -lmassv -lm -qsmp=omp								
	// O5								
	replace -O3 with -O5								
	All timings are in seconds								
		CASE	**Crystal_div**	**Crystal_div_mass**	**Crystal_pow**	**Crystal_pow_mass**	**Crystal_Cholesky**		
	P5	O3	2.328	2.1860	2.9835	7.0975	4.8714		

			506	43	1	2E-01	46		
		O5	2.333469	2.186085	2.968783	9.19594E-01	4.874775		
	P7	O3	1.330957	1.341726	0.608134	4.30709E-01	2.360153		
		O5	1.321914	1.326606	0.60717	4.25724E-01	2.294489		
		SPEED UP P5/P7							
		O3	1.75	1.63	4.91	1.65000E+00	2.06		
		O5	1.77	1.65	4.89	2.16000E+00	2.12		
		SPEEDUP for _mass							
	P5	O3		1.07		4.20000E+00			
		O5		1.07		3.23000E+00			
	P7	O3		0.99		1.41000E+00			
		O5		1		1.43000E+00			
P5_P7.IRS									
	Date : 10/2010								
	Base line:								
	Running on pdev(power5)								
	Compilation line:								
	//***** P5 1.9GHz								
	// O3								
	CFLAGS = -c -qlanglvl=stdc99 -O3 -qhot -qalias=allp -qtune=auto -qarch=auto -qcache=auto -qsmp=omp -qmaxmem=16384								
	LDFLAGS = -blpdata -lm -qsmp=omp								

	// O5								
	replace -O3 with -O5								
	//***** P7 3.36GHz 1.77XP5								
	// O3								
	CFLAGS = -c -O3 -qhot -qsimd=auto -qhot=novector -qalias=allp -qarch=auto -qtune=auto -qcache=auto -qsmp=omp -qlanglvl=stdc99 -qmaxmem=16384								
	LDFLAGS = -blpdata -lm -qsmp=omp								
	// O5								
	replace -O3 with -O5								
	noIter = 5000								
	All timing are in seconds								
	rmatmult3_old : orig. version								
	rmatmult3_p5_vx : version target for no. of prefectch streams on P5								
	rmatmult3_p7 : version target for no. of prefectch streams on P7								
			CASE/iter	**rmatmult3_old**	**rmatmult3_p5_v1**	**rmatmult3_p5_v2**	**rmatmult3_p7**		
	P5	O3							
			25	6.184263	2.396684	2.40692E+00			
			50	48.194554	18.471385	1.84474E+01			
			100	579.151223	200.398553	1.86360E+02			
		O5							
			25	6.191328	2.397685	2.40419E+00			
			50	48.075	18.440	1.8429			

				916	049	0E+01			
			100	571.096963	204.945528	2.07237E+02			
	P7	O3							
			25	2.573418			2.933024		
			50	28.328686			26.33407		
			100	188.685525			106.2636		
		O5							
			25	2.672409			3.015162		
			50	28.751782			36.29694		
			100	183.09343			104.6409		
		/***** P5/P7 speedup							
		O3							
			25	2.4					
			50	1.7					
			100	3.1					
		O5							
			25	2.3					
			50	1.7					
			100	3.1					
		/***** P7 rmatmult3_old vs rmatmult3_p7 speedup							
		O3							
			25	0.88					
			50	1.08					
			100	1.78					
		O5							
			25	0.89					
			50	0.79					
			100	1.75					

P5_P7.UMT									
	1) later version								
	2) automatic control flow								
	3) C version								
	Date : 10/2010								
	Base line:								
	Running on pdev(power5)								
	Compilation line:								
	//***** P5 1.9GHz								
	// O3								
	FFLAGS = -c -O3 -qhot -qarch=auto -qtune=auto -qcache=auto -qsmp=omp -qnosave -qfree=f90 -qsuffix=cpp=F90								
	CFLAGS = -c -O3 -qhot -qalias=allp -qarch=auto -qtune=auto -qcache=auto -qsmp=omp -qlanglvl=stdc99								
	LDFLAGS = -blpdata -qsmp=omp								
	// O5								
	replace -O3 with -O5								
	//***** P7 3.36GHz 1.77XP5								
	FFLAGS = -c -O3 -qhot -qsimd=auto -qhot=novector -qarch=auto -qtune=auto -qcache=auto -qsmp=omp -qnosave -qfree=f90 -qsuffix=cpp=F90								
	CFLAGS = -c -O3 -qhot -qsimd=auto -qhot=novector -qalias=allp -qarch=auto -qtune=auto -qcache=auto -qsmp=omp -qlanglvl=stdc99								
	// O5								
	replace -O3 with -O5								
	All timing are in seconds								
			CASE/iter	**1/400000**	**2/500000**	**3/250000**			
	P5	O3							
			F	6.00E-01	3.15E-01	6.63810E-01			
			C	1.30E+	3.85E-	1.2361			

				00	01	8E+00			
		O5							
			F	5.87E-01	3.12E-01	6.53630E-01			
			C	1.29E+00	9.75E-01	1.33851E+00			
	P7	/***** NO -qsimd=auto							
		O3							
			F	3.01E-01	1.68E-01	3.17610E-01			
			C	2.91E-01	1.66E-01	3.23361E-01			
		O5							
			F	4.92E-01	9.22E-01	6.65430E-01			
			C	4.86E-01	9.17E-01	6.73228E-01			
		SPEED UP P5/p7							
		O3							
			F	1.99	1.87	2.09000E+00			
			C	4.45	2.32	3.82000E+00			
		O5							
			F	1.19	0.34	9.80000E-01			
			C	2.65	1.06	1.99000E+00			
	P7	/***** -qsimd=auto							
		bgq bgq restructure // -O3 1.87x -O5 3.39x(with sligth code change) vs scalar							
		v1 scalar optimization							
		v2 vectorization							
			CASE/iter	**1/400000**	**2/500000**	**3/250000**			
		O3							

		F							
				2.22E-01	1.51E-01	2.55310E-01			
			bgq	2.23E-01	1.45E-01	2.43010E-01			
			v1	2.14E-01	1.48E-01	2.40600E-01			
			v2	2.17E-01	1.51E-01	2.37150E-01			
		C		2.28E-01	1.45E-01	2.51186E-01			
		O5							
		F							
				2.31E-01	1.49E-01	2.56670E-01			
			bgq	3.68E-01	1.48E-01	3.67380E-01			
			v1	2.15E-01	1.47E-01	2.42550E-01			
			v2	2.18E-01	1.49E-01	2.38180E-01			
		C		2.34E-01	1.46E-01	2.61039E-01			
		SPEEDUP compare without simd							
		O3							
		F		1.36	1.11	1.24000E+00			
		C		1.28	1.15	1.29000E+00			
		O5							
		F		2.13	6.19	2.59000E+00			
		C		2.08	6.26	2.58000E+00			
	P7	/***** !IBM* stream_unroll(n)							
		O3							
		F	!IBM*	stream_unroll(					

				2)					
				2.2117 0E-01	1.4764 0E-01	2.5221 0E-01			
			bgq	2.2112 0E-01	1.4513 0E-01	2.4296 0E-01			
			v1	2.1341 0E-01	1.4776 0E-01	2.3757 0E-01			
			v2	2.1419 0E-01	1.4759 0E-01	2.3728 0E-01			
		F	!IBM*	stream _unroll(4)					
				2.2301 0E-01	1.4756 0E-01	2.5227 0E-01			
			bgq	2.2028 0E-01	1.4511 0E-01	2.4304 0E-01			
			v1	2.1434 0E-01	1.4760 0E-01	2.3748 0E-01			
			v2	2.1420 0E-01	1.4785 0E-01	2.3831 0E-01			
		F	!IBM*	stream _unroll(8)					
				2.2126 0E-01	1.4746 0E-01	2.5225 0E-01			
			bgq	2.2034 0E-01	1.4511 0E-01	2.4398 0E-01			
			v1	2.1532 0E-01	1.4758 0E-01	2.3747 0E-01			
			v2	2.1312 0E-01	1.4765 0E-01	2.3741 0E-01			
		O5							
		F	!IBM*	stream _unroll(2)					
				2.3016 0E-01	1.4913 0E-01	2.5664 0E-01			
			bgq	3.6914 0E-01	1.4735 0E-01	3.6442 0E-01			
			v1	2.1379 0E-01	1.4634 0E-01	2.4191 0E-01			
			v2	2.1813 0E-01	1.4929 0E-01	2.3861 0E-01			
		F	!IBM*	stream _unroll(4)					

				2.2702 0E-01	1.4881 0E-01	2.5668 0E-01			
			bgq	3.6598 0E-01	1.4756 0E-01	3.6415 0E-01			
			v1	2.1385 0E-01	1.4625 0E-01	2.3873 0E-01			
			v2	2.1493 0E-01	1.4620 0E-01	2.3845 0E-01			
		F	!IBM*	stream _unroll(8)					
				2.2695 0E-01	1.4916 0E-01	2.5608 0E-01			
			bgq	3.6722 0E-01	1.4744 0E-01	3.6437 0E-01			
			v1	2.1387 0E-01	1.4642 0E-01	2.3875 0E-01			
			v2	2.1455 0E-01	1.4657 0E-01	2.3849 0E-01			
	Note:								
	1) P7 without SIMD speedup factor greater than the clock speedup factor which is								
	extremely good. That implies the compiler is doing a very good job especailly in C.								
	It may explains why other restructure has mim. effect.								
	2) unroll did not enhance simd as BGQ does								
	3) For v2								
	-c -O3/05 -qhot -qsimd=auto -qhot=novector -qarch=auto -qtune=auto -qcache=auto -qsmp=omp -qnosave -qfree=f90 -qsuffix=cpp=F90 -qreport								
	original timing 0.22182E+00								
	//***** call vrec(t_array,t_array,Groups)								
	Both O3/O5								
	3.10E-01								
	//******								

	do ig=1,Groups								
	t_array(ig) = 1/t_array(ig)								
	enddo								
	Both O3/O5								
	4.28E-01								
	//******								
	one big loop								
	2.14E-01								
P7_BG.CAM									
	Date : 12/1/2010								
	//***** P7 3.36GHz 1.77XP5								
	// O3								
	FFLAGS = -c -O3 -qhot -qsimd=auto -qhot=novector -qarch=auto -qtune=auto -qcache=auto -qsmp=omp -qnosave -qfree=f90 -qsuffix=cpp=F90								
	CFLAGS = -c -O3 -qhot -qsimd=auto -qhot=novector -qalias=allp -qarch=auto -qtune=auto -qcache=auto -qsmp=omp -qlanglvl=stdc99								
	LDFLAGS = -blpdata -qsmp=omp								
	// O5								
	replace -O3 with -O5								
	All timings are in seconds								
	P7 DAWN								
	no simd simd nosimd/simd								
test case	**n/im**	**0.00000E+00**	**0**	**0**	**0**	**3**	**5**	**nosimd/simd**	
CAM_dyn_c_sw_k1	9/1152	1.50E-05	1.19E-05	1.19200E-05	1.10E-05	1.26	1.09	2	*
CAM_dyn_c_sw_k2		6.20E-06	6.20E-06	6.19900E-06	6.20E-06	1	1	2	

CAM_dyn_c_sw_k3		3.38E-02	3.41E-02	3.55700E-02	3.48E-02	0.95	0.98	1.5	
CAM_dyn_c_sw_k4		6.55E-02	6.57E-02	4.62300E-02	4.58E-02	1.42	1.43	1.6	*
CAM_dyn_c_sw_k5		5.20E-03	5.22E-03	2.67700E-03	2.69E-03	1.94	1.94	1.6	* <--
CAM_dyn_c_sw_k6		9.06E-06	9.06E-06	8.82100E-06	9.30E-06	1.03	0.97	1.2	
CAM_dyn_c_sw_k7		1.17E-05	1.14E-05	1.14400E-05	1.12E-05	1.02	1.02	1.4	
CAM_dyn_c_sw_k8		2.95E-02	2.93E-02	2.68600E-02	2.71E-02	1.1	1.08	1.8	*
CAM_dyn_tp2d_k1		3.45E-02	3.41E-02	3.67000E-02	3.89E-02	0.94	0.88	1.2	
CAM_dyn_tp2d_k2		3.00E-05	3.15E-05	2.83700E-05	3.17E-05	1.06	0.99	1	* <--
CAM_dyn_xtpv_k1		7.76E-02	9.29E-02	7.42900E-02	7.40E-02	1.04	1.26	1	* <--
CAM_dyn_fxppm_k1	1/1152	2.31E-02	2.31E-02	2.28700E-02	2.27E-02	1.01	1.02	1	

CAM_dyn_fxppm_k2		6.48E-03	3.91E-03	3.94100E-03	4.00E-03	1.64	0.98	1	* <--
CAM_dyn_lmppm_k1		4.13E-02	4.12E-02	4.12900E-02	4.12E-02	1	1	0.9	
CAM_dyn_d_sw_k1		5.14E-02	5.14E-02	2.38400E-07	2.38E-07	N/A		1	
CAM_remap_map1_ppm_	30/160	2.15E-02	2.15E-02	2.27700E-02	2.28E-02	0.94	0.94	1.1	
CAM_remap_ppm2m_k1		6.28E-02	6.28E-02	6.98400E-02	7.02E-02	0.9	0.89	1.3	
CAM_remap_ppm2m_k2		6.70E-05	6.72E-05	6.72300E-05	6.72E-05	1	1	1.2	
CAM_remap_ppm2m_k3		2.86E-06	1.08E-03	2.86100E-06	1.09E-03	1	0.99	1.1	
CAM_remap_ppm2m_k4		4.47E-02	4.47E-02	8.64800E-02	8.57E-02	0.52	0.52	1	
CAM_remap_kmppm_k1		9.67E-02	9.66E-02	8.65200E-02	8.66E-02	1.12	1.12	0.9	* <--
	Note:								
	1) * means some speedup								
	2) <-- means perform better than BG among *								
	3) overall BG performs								

	better								
P7_BG.MF24									
	Date : 12/1/2010								
	//***** P7 3.36GHz 1.77XP5								
	// O3								
	FFLAGS = -c -O3 -qhot -qsimd=auto -qhot=novector-qarch=auto -qtune=auto -qcache=auto -qsmp=omp -qnosave -qfree=f90 -qsuffix=cpp=F90								
	CFLAGS = -c -O3 -qhot -qsimd=auto -qhot=novector -qalias=allp -qarch=auto -qtune=auto -qcache=auto -qsmp=omp -qlanglvl=stdc99								
	LDFLAGS = -blpdata -qsmp=omp								
	// O5								
	replace -O3 with -O5								
	vector lenght n = 1024 // other n = 16,64,256 available upon request								
	All timings are in seconds								
	no simd		simd						nosimd/simd
		P7		**DAWN**					
	test case	**-O3 F/c**	**-O5 F/c**	**-O3 F/c**	**-O5 F/c**	**03**	**05**	**nosimd/simd**	
	k1	0.95367E-06/	0.11921E-05/	0.95367E-06/	0.11921E-05/	1	1	1.41	
		9.54E-07	1.19E-06	1.19E-06	9.53674E-07	0.8	1.25	1.04	* <--
	k2	0.78843E+00/	0.78857E+00/	0.78675E+00/	0.78699E+00/	1	1	1	
		7.87E-01	7.88E-01	7.89E-01	7.87107E-01	1	1	1	
	k3	0.36639E+00/	0.36637E+00/	0.45792E+00/	0.45798E+00/	0.8	0.8	1.48	
		6.11E-	6.11E-	4.58E-	4.5792	1.33	1.33	0.89	*

		01	01	01	7E-01				<--
	k4	0.18286E+00/	0.18434E+00/	0.18452E+00/	0.18385E+00/	0.99	1	1	
		2.89E-01	2.89E-01	2.88E-01	2.88096E-01	1	1	0.79	
	k5	0.54860E+00/	0.54708E+00/	0.54686E+00/	0.54687E+00/	1	1	1	
		5.64E-01	5.64E-01	5.64E-01	5.64505E-01	1	1	1	
	k6	0.87931E+00/	0.86490E+00/	0.87115E+00/	0.86108E+00/	1.01	1	0.69	
		8.81E-01	8.65E-01	8.88E-01	8.78905E-01	0.99	0.98	1	
	k7	0.21458E-05/	0.23842E-05/	0.21458E-05/	0.23842E-05/	1	1	1.22	
		2.86E-06	2.38E-06	2.38E-06	2.38419E-06	1.2	1	1	* <--
	k8	0.45362E+00/	0.44503E+00/	0.43003E+00/	0.42617E+00/	1.05	1.05	1.49 *	
		6.41E-01	6.41E-01	6.45E-01	6.41658E-01	0.99	1	1	
	k9	0.42915E-05/	0.40531E-05/	0.24840E+00/	0.24831E+00/	N/A		0.88	
		4.05E-06	4.05E-06	6.45E-01	6.44777E-01				
	k10	0.21933E+00/	0.21928E+00/	0.65426E+00/	0.65467E+00/	0.34	0.33	1	
		2.44E-01	2.44E-01	6.59E-01	6.59523E-01	0.37	0.37	1	
	k11	0.54502E+0	0.54485E+0	0.54465E+00/	0.54593E+00/	1	1	1	

		0/	0/						
		5.46E-01	5.46E-01	5.46E-01	5.45692E-01	1	1	1	
	k12	0.47684E-06/	0.71526E-06/	0.47684E-06/	0.71526E-06/	1	1	1.49	
		4.77E-07	7.15E-07	4.77E-07	4.76837E-07	1	1.5	1	* <--
	k13	0.56072E+00/	0.56214E+00/	0.54093E+00/	0.54085E+00/	1.04	1.04	1	* <--
		5.88E-01	5.88E-01	5.26E-01	5.25936E-01	1.12	1.12	1	* <--
	k14	0.30958E+00/	0.30949E+00/	0.21499E+00/	0.21462E+00/	1.44	1.44	1	* <--
		2.86E-01	2.80E-01	2.11E-01	2.11358E-01	1.35	1.32	1	* <--
	k15	0.59170E+00/	0.59354E+00/	0.59347E+00/	0.59348E+00/	1	1	1.11	
		5.65E-01	5.68E-01	5.59E-01	5.77648E-01	1.01	0.98	1.06	
	k16	0.53008E+00/	0.53383E+00/	0.56717E+00/	0.56551E+00/	0.93	0.94	0.88	
		4.16E-01	4.60E-01	4.68E-01	4.70562E-01	0.89	0.98	1	
	k17	0.44963E+00/	0.45433E+00/	0.49200E+00/	0.59994E+00/	0.91	0.76	1	
		4.61E-01	4.73E-01	5.97E-01	5.97549E-01	0.77	0.79	0.96	
	k18	0.58000E+00/	0.58317E+00/	0.46779E+00/	0.46024E+00/	1.24	1.27	1.3	*
		5.87E-01	5.86E-01	4.68E-01	4.45589E-01	1.25	1.31	1	* <--

	k19	0.73263E+00/	0.73263E+00/	0.73259E+00/	0.73262E+00/	1	1	1	
		7.33E-01	7.33E-01	7.33E-01	7.32619E-01	1	1	1	
	k20	0.56071E+00/	0.56057E+00/	0.56354E+00/	0.56359E+00/	0.99	0.99	1	
		5.40E-01	5.40E-01	5.45E-01	5.45219E-01	0.99	0.99	1	
	k21	0.28681E-01/	0.12888E-01/	0.28409E-01/	0.12948E-01/	1.01	0.99	1	
		1.35E-02	1.27E-02	1.01E-02	9.18698E-03	1.33	1.38	1	* <--
	k22	0.25749E-04/	0.25272E-04/	0.25988E-04/	0.25749E-04/	0.99	0.98	1	
		2.43E-05	2.43E-05	2.38E-05	2.45571E-05	1.02	0.99	1	
	k23	0.54891E+00/	0.54903E+00/	0.54892E+00/	0.54912E+00/	1	1	1	
		5.49E-01	5.49E-01	5.49E-01	5.49346E-01	1	1	1	
	k24	0.11529E+01/	0.11001E+01/	0.12564E+01/	0.11357E+01/	0.92	0.97	0.88	
		4.18E-01	4.24E-01	4.18E-01	4.18612E-01	1	1.01	1	
	Note:								
	1) * means some speedup								
	2) <-- means perform better than BG among *								
P5_P7.EPCC									
	Base line:								
	Running on								

	pdev(power5)								
	Compilation line:								
	CFLAGS = -c -O3 -qhot -qalias=allp -qarch=auto -qtune=auto -qcache=auto -qsmp=omp -qlanglvl=extc99								
	LDFLAGS = -blpdata -qsmp=omp								
	Env.								
	export XLSMPOPTS=spins=0:yields=0								
	//***** P7 3.36GHz 1.77XP5								
	All timings are in microseconds								
	Timing are for *overhead*								
		2ths		**4ths**		**8ths**			
	test case	**P5**	**P7**	**P5**	**P7**	**P5**	**P7**		
	PARALLEL	1.90166	1.684711	3.248097	3.127009	1.06520E+01	4.527183		
	DD2.0		1.916038		2.728317		4.545606		
			1.848595		2.848529		4.355562		
	FOR	2.518771	1.27208	3.527094	3.078789	5.47109E+00	5.878313		
			1.443325		2.446077		6.164361		
			1.201098		3.391825		5.517864		
	PARALLEL FOR	2.401159	1.624451	3.849722	3.330511	5.58812E+00	4.88102		
			1.893984		3.19278		4.81285		
			1.893501		3.176068		4.649711		
	BARRIER	0.769088	0.442884	1.00515	0.95343	1.46213E+00	1.201661		
			0.514578		0.736604		1.078178		

			0.520198		0.769745		1.113069		
	SINGLE	0.271568	0.148306	0.33492	0.602859	7.41677E-01	1.336713		
			0.194858		0.591383		1.391281		
			0.171177		0.248681		1.020312		
	CRITICAL	0.283421	0.472939	0.346874	0.929587	3.66574E-01	1.600826		
			0.735822		0.928999		1.566212		
			0.547886		0.876593		1.52034		
	LOCK/UNLOCK	0.167524	0.44898	0.200047	0.922738	2.20197E-01	1.570888		
			0.748969		0.93747		1.538556		
			0.527862		0.873474		1.495963		
	ORDERED	0.399146	0.311694	0.452043	0.363129	5.35135E-01	0.431664		
			0.355374		0.325034		0.407435		
			0.360684		0.33177		0.394809		
	ATOMIC	0.117996	0.254076	0.260021	0.764055	3.99907E-01	1.560864		
			0.32686		0.849774		1.551893		
			0.246389		0.828306		1.531153		
	REDUCTION	2.132506	1.898651	3.569279	3.47002	5.38495E+00	5.0862		
			1.967902		2.863342		4.802102		
			1.933898		2.936732		4.571909		
	Assumed clock rate								

	1900 MHz 3360 MHz								
		2ths		**4ths**		**8ths**			
	test case	**P5**	**P7**	**P5**	**P7**	**P5**	**P7**		
	STATIC	2.051294	1.594567	3.361821	3.14131E+00	7.135952	6.126773		
	DD2.0		1.42101		3.01286E+00		6.278384		
			1.102841		3.80573E+00		5.626798		
	STATIC 1	18.915832	12.349153	32.178211	2.88891E+01	48.786557	44.93363		
			9.893894		2.99216E+01		42.32864		
			11.552799		3.03786E+01		41.61562		
	STATIC 2	9.740627	8.814192	15.6636	1.62618E+01	25.213635	25.6026		
			7.162297		1.33785E+01		23.04075		
			7.220566		1.44237E+01		23.43073		
	STATIC 4	5.888569	6.784213	7.756495	7.74602E+00	13.036978	15.65301		
			7.092237		6.14516E+00		13.2995		
			7.078683		7.09040E+00		14.34052		
	STATIC 8	3.793812	3.026521	5.27589	4.86805E+00	7.722831	9.679151		
			2.78703		4.35115E+00		8.709085		
			3.121746		5.04125E+00		8.498216		
	STATIC 16	2.809644	2.261674	4.129624	3.89996E+00	6.527126	7.212925		
			2.104712		3.63421E+00		7.116401		
			2.419758		4.24889E+00		6.704438		

	STATIC 32	2.348399	1.880443	3.605783	3.45455E+00	6.115985	6.549132		
			1.758361		3.32048E+00		6.616759		
			2.058578		3.92655E+00		6.267273		
	STATIC 64	2.119505	1.682484	3.589332	3.25582E+00	5.815911	6.394351		
			1.581025		3.13228E+00		6.747103		
			1.915717		3.72108E+00		6.067657		
	STATIC 128	2.073944	1.576686	3.416967	3.16283E+00	5.668497	6.191742		
			1.475763		3.12040E+00		6.35221		
			1.816869		3.68420E+00		5.953419		
	DYNAMIC 1	64.798427	46.712875	153.201056	4.34456E+02	452.10815	1638.998		
			45.95505		5.12483E+02		1715.126		
			41.674471		4.38267E+02		1584.585		
	DYNAMIC 2	29.188836	35.472822	76.419139	2.19006E+02	228.24173	833.2816		
			19.557691		2.59705E+02		874.9554		
			19.622457		2.17432E+02		812.0256		
	DYNAMIC 4	14.425886	9.966505	46.847069	1.13192E+02	131.6797	420.0491		
			8.834016		1.36766E+02		442.7755		
			8.455575		1.16490E+02		413.101		
	DYNAMIC 8	5.480707	4.657495	22.460532	5.75961E+01	72.0499	214.5207		
			3.668		6.8599		225.28		

			392		0E+01		61		
			3.754878		5.90224E+01		209.7616		
	DYNAMIC 16	3.054917	2.333307	7.538629	3.01405E+01	33.94806	112.2857		
			2.182221		3.60954E+01		118.2332		
			2.170157		3.10055E+01		109.5829		
	DYNAMIC 32	2.038908	1.515555	3.317833	1.52498E+01	12.78334	60.76235		
			1.453638		1.74042E+01		63.55588		
			1.50311		1.56315E+01		59.11999		
	DYNAMIC 64	1.482737	1.132643	2.858698	6.07221E+00	5.3635	32.40244		
			1.133525		7.06907E+00		33.6274		
			1.535022		6.34897E+00		31.01714		
	DYNAMIC 128	1.268578	0.93025	2.893615	4.15241E+00	5.17088	15.74007		
			0.899029		4.79563E+00		16.66117		
			1.024401		4.31070E+00		14.76507		
	GUIDED 1	4.87628	5.929172	12.822092	4.22312E+01	41.13541	158.516		
			6.960547		6.34718E+01		213.3603		
			4.586816		3.67585E+01		133.9801		
	GUIDED 2	3.364742	4.66435	9.750092	2.97745E+01	31.31334	115.4242		
			4.772222		4.16545E+01		143.6207		
			4.001141		2.72684E+01		101.9759		

	GUIDED 4	2.615678	3.080142	8.405089	2.25067E+01	25.65813	85.32546		
			3.209567		2.99242E+01		101.4899		
			3.100812		2.15764E+01		79.53399		
	GUIDED 8	1.757371	2.525842	6.638587	1.78503E+01	22.79102	69.57107		
			2.361774		2.19332E+01		76.82293		
			2.482569		1.75006E+01		65.76092		
	GUIDED 16	1.692593	1.931942	4.682589	1.47117E+01	16.1761	56.78276		
			1.480556		1.74028E+01		61.62913		
			1.821554		1.45426E+01		54.59787		
	GUIDED 32	1.549172	1.175451	3.237963	1.03421E+01				
			1.211512		1.15224E+01				
			1.555967		9.80855E+00				
	GUIDED 64	1.430082	1.090407						
			1.09731						
			1.3183						
P5_P7.Matrix									
	Compilation line:								
	//***** P5								
	FFLAGS = -c -O3 -qhot -qarch=auto -qtune=auto -qcache=auto -qsmp=omp -qnosave -qfree=f90 -qsuffix=cpp=F90								
	//***** P7								
	FFLAGS = -c -O3 -qhot -qsimd=auto -qhot=novector -qarch=auto -qtune=auto -qcache=auto -qsmp=omp -qnosave -qfree=f90 -qsuffix=cpp=F90 -qreport								

		P5	**P7**	**P7/P5**					
	clock	1.9GHz	3.36GHz	1.77					
	Execution time (wall clock time) second	2.033502	0.7436386 09	0.366					
	Processor cycles(PM_CYC)	3307768579	2355144408	0.712					
	Instructions completed(PM_INST_CMPL)	6511536783	3064924701	0.471					
	Instructions per cycle	1.969	1.301	0.661					
	MIPS	3186.215 MIPS	4169.044 MIPS	1.309					
	Instruction mix:								
	Total Load								
	L1 D cache load references(PM_LD_REF_L1)	1868600370	574517880	0.307					
	Total Store								
	L1 D cache store reference(PM_ST_REF_L1	1198398299							
	PM_ST_FIN (Store Instructions Finished)		351222855	0.293					
	Load+Store done by LSU								
	FOR P5 PM_LD_REF_L1 + PM_ST_REF_L1 - PM_FPU_STF								

		1868600370 + 1198398299 - 1008102228 2058896441							
	PM_LSU_FIN (LSU Finished an instruction (up to 2 per cycle)):								
			1021233806	0.496					
	Floating Point load								
	LSU executed Floating Point load instruction			1661407489					
	(PM_LSU_LDF)								
	PM_LSU_LDF (All Scalar Loads)			23915779					
	PM_LSU_LDX (All Vector loads (vsx vector + vmx vector))				487806725				
	FOR P7 Total Floating Point load								
	PM_LSU_LDF + PM_LSU_LDX								
			511722504	0.308					
	FXU								
	FXU produced a result(PM_FXU_FIN)								
		1058501896	822876900	0.777					
	Branch								
	Branches issued(PM_BR_ISSUED)			152234136					
	PM_BRU_FIN (Branch Instruction Finished)								
			64365871	0.423					
	[ ] % of BR Miss Prediction			5.67%					
	FPU								
	FPU produced a result(PM_FPU_FIN)			3505674587					
	PM_VSU_FIN (VSU0 Finished an instruction)								

			1574272625	0.449					
	FPU executed FDIV instruction(PM_FPU_FDIV)			3000125					
	hardly any FSQRT in UMT								
	PM_VSU_FSQRT_FDIV								
			3000055	1					
	PM_VSU_FSQRT_FDIV_DOUBLE (DP vector versions of fdiv,fsqrt)								
				35200038					
	P5 use FMA to do double FDIV?								
	FPU executed multiply-add instruction(PM_FPU_FMA)								
				1248003526					
	PM_VSU_FMA			702					
	PM_VSU_FMA_DOUBLE								
			278400854	0.223					
	FPU executed store instruction(PM_FPU_STF)			1008102228					
	PM_VSU_STF (FPU store (SP or DP) issued on Pipe0)								
				29936352					
	PM_VSU1_SQ (Store Vector Issued on Pipe1)								
			284532437	0.312					
	PM_FPU_FEST (FPU executed FEST instruction)			17578276					
	PM_FLOP (Floating Point Operation Finished)			1038749323					
	PM_VSU_1FLOP			53346004					
	PM_VSU_2FLOP			668802421					
	PM_VSU_2FLOP_DOUBLE			668801722					
	PM_VSU_4FLOP			281400787					
	PM_VSU_8FLOP			35200044					
	Cache and TLB:								

	Load								
	L1 D cache load references(PM_LD_REF_L1)								
		1868600370	574138212	0.307					
	L1 D cache load misses(PM_LD_MISS_L1)								
		377526	359164	0.951					
	Data TLB misses(PM_DTLB_MISS)			136414					
	PM_DTLB_MISS (TLB reload valid)								
			5304	0.039					
	Number of loads per DTLB miss								
		13670.972	1082469.269	7.919					
	PM_LD_REF_L1/ PM_DTLB_MISS								
	number of loads per load miss								
		4625.197	1599	0.346					
	PM_LD_REF_L1/PM_LD_MISS_L1								
	Store								
	L1 D cache store reference(PM_ST_REF_L1)			1198398299					
	PM_ST_FIN (Store Instructions Finished)								
			349879023	2.92000E-01					
	L1 D cache store misses(PM_ST_MISS_L1)								
		53075431	52661557	9.92000E-01					
	number of stores per store miss								
		22.5	6.64	2.95000E-01					
	PM_ST_REF_L1/PM_ST_MISS_L1								
	Percentage of L1 store misses per L1 store	ref		17.81%					
	Floating Point:		Group Set						
	Theroretical floating-point peak 1.9GHz * 2(FPU)* 2(FMA) 3.36 * 2(vector) * 2(FMA)								
		7.6GF		1.77					

			13.44F GF						
	HW Float point instructions	per Cycle							
		1.969	1.301	0.66					
	Wall Clock Time								
		2.033 502	0.743 638609	0.366					
	Flip								
	P5								
	PM_FPU_FIN + PM_FPU_FMA - PM_FPU_STF - PM_FPU_FEST								
	3505674587 + 1248003526 - 1008102228 - 17578276				3727997609				
	P7								
	PM_FPU_FIN + PM_VSU_FMA_DOUBLE + PM_VSU_FMA - PM_VSU_STF - PM_VSU1_SQ								
	1574272625 + 278400854 + 702 - 29936352 - 284532437				1538205392				
	P7/P5				4.13000E-01				
	flip/sec								
	flip/WCT	1833 M	2069 M	1.13					
	FMA %								
	100 * PM_FPU_FMA * 2 / flip								
		67	36	0.54					
	Branches:								
	Branches issued(PM_BR_ISSUED)			152234136					
	Branch mispredictions due to CR bit	setting		12377244					
	(PM_BR_MPRED_CR)								
	Branch mispredictions due to target	address		8487					
	(PM_BR_MPRED_TA)								

	PM_BRU_FIN (Branch Instruction Finished)								
			64365871	0.423					
	PM_BR_PRED (Branch Predictions made)			60500952					
	PM_BR_MPRED (Number of Branch Mispredicts)								
				3428832					
	PM_BR_MPRED_CR (Branch mispredict - taken/not taken)								
			1191946	0.096					
	PM_BR_MPRED_TA (Branch mispredict - target address)								
			4761	0.561					
	PM_BR_MPRED_CCACHE			1139					
	(Branch Mispredict due to Count Cache prediction)								
	PM_BR_MPRED_LSTACK (Branch Mispredict due to Link Stack)								
				3547					
	Stalls:								
	Run cycles(PM_RUN_CYC)								
		3307768579	2355144408	0.712					
	Completion stall caused by LSU instruction								
		242842766	148847113	0.613					
	(PM_CMPLU_STALL_LSU)								
	Completion stall caused by D cache miss								
		5653192	15089638	2.67					
	(PM_CMPLU_STALL_DCACHE_MISS)								
	Completion stall caused by FXU instruction								
		266912285	117012695	0.438					
	(PM_CMPLU_STALL_FXU)								
	Completion stall caused by FPU								

	instruction								
				812246689					
	(PM_CMPLU_STALL_FPU)								
	PM_CMPLU_STALL_SCALAR		:	130317948					
	(Completion stall caused by FPU instruction)								
	PM_CMPLU_STALL_VECTOR		:	949474458					
	(Completion stall caused by Vector instruction)								
	Total for P7		1079792406	1.33					