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Performance of a 512 x 512 Gated CMOS Imager with a 250 ps Exposure Time

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ABSTRACT

We describe the performance of a 512x512 gated CMOS read out integrated circuit (ROIC) with a 250 ps exposure time. A low-skew, H-tree trigger distribution system is used to locally generate individual pixel gates in each 8x8 neighborhood of the ROIC. The temporal width of the gate is voltage controlled and user selectable via a precision potentiometer. The gating implementation was first validated in optical tests of a 64x64 pixel prototype ROIC developed as a proof-of-concept during the early phases of the development program. The layout of the H-Tree addresses each quadrant of the ROIC independently and admits operation of the ROIC in two modes. If "common mode" triggering is used the camera provides a single 512x512 image. If independent triggers are used, the camera can provide up to 4 256x256 images with a frame separation set by the trigger intervals. The ROIC design includes small (sub-pixel) optical photodiode structures to allow test and characterization of the ROIC using optical sources prior to bump bonding. Reported test results were obtained using short pulse, second harmonic Ti:sapphire laser systems operating at $\lambda \sim 400$ nm at sub-ps pulse widths.

Keywords: Gated imagers, x-ray imagers, CMOS imagers

I. INTRODUCTION

X-ray imaging instruments are ubiquitous diagnostics for high energy density physics experiments. At NIF, x-ray imagers are used routinely to measure laser entrance hole (LEH) closure[1], obtain time-resolved images of imploding cores[2], radiograph dynamic processes at high density[3] and record dynamic diffraction patterns in materials science experiments[4]. Future experiments at NIF would benefit from multiple frame (8 or more) single line of sight x-ray imaging detectors capable of producing megapixel images, at 20 μm spatial resolution with user selectable gate durations adjustable over a range spanning 10 – 1000 ps, recording x-ray images over a range of x-ray energies spanning 1 – 50 keV.

Virtually all of these projected applications require multiple frames along a single line-of-sight; however, additional requirements on energy range, frame rate, gate width, sensor response time are application specific. It is difficult to satisfy all of these requirements in a single embodiment of an imaging sensor. We have adopted a development approach which admits the use of a common-platform for sensor readout; application specific embodiments are engineered by integrating the ROIC with customized sensors tailored to meet each experimental requirement.

This development was undertaken as a Lawrence Livermore National Laboratory (LLNL) and Massachusetts Institute of Technology Lincoln Laboratory (MIT-LL) collaboration that leveraged MIT-LL expertise in solid state imaging technology and LLNL expertise in both High Energy Density Science and high speed detection. In the phase I program a 64x64 pixel prototype ROIC[5], supporting electronics and control software was designed and fabricated to permit experimental testing and validation of the conceptual design. The 64x64 pixel prototype ROIC included photodiode structures in each pixel that enabled dynamic testing using short pulse laser excitation of the internal photo-diodes. A critical issue for these imagers is providing a low-skew trigger across the ROIC. In our prototype design, an H-Tree trigger distribution system provides each 8x8 group of pixels (neighborhood) with a trigger input, and the sampling gates are generated locally utilizing on chip processing of the trigger signal within each neighborhood. The validated concepts were used in the design of the phase II implementation, a 512x512 imager.

The 512x512 ROIC is actually comprised of four 256x256 quadrants. Triggers for each quadrant are generated via an H-Tree structure, identical to that discussed above; however, the major H-Tree in each quadrant can be triggered

independently. Therefore, the camera is capable of providing up to 4 256x256 images. Alternatively the quadrant H-trees can be triggered simultaneously to provide a single 512x512 image. Each pixel of the ROIC also included an internal photo-diode which enables qualification of each ROIC prior to bump-bonding the application specific sensors. The ROICs were fabricated at the TSMC foundry using a 0.18 mm CMOS process. The experimental results presented herein were obtained using a frequency doubled Ti:sapphire system to excite the on-chip photo-diodes.

The development of bump-bonded Si photodiode sensor arrays for the 512x512 imager was launched in parallel with the camera design. A major challenge for this technology is developing a sensor arrays capable of handling the large current loads induced by x-ray exposure during a NIF imaging experiment. The engineering design achieves this by sacrificing a fraction of the sensor pixels to install through wafer vias, back-filled with metal, to provide efficient current return and reduce the sensor impedance from 60 to 0.002 Ω.

II. 64 x 64 TEST READOUT INTEGRATED CIRCUIT

In order to validate the concepts for the variable gating and trigger distribution MIT-LL designed and fabricated a 64x64 pixel test ROIC[5]. The ROIC was mounted in a standard holder and a custom electronic readout board was fabricated. Gate pulses are generated by circuitry in each 8x8 neighborhood and shutter exposure time is adjusted with the voltage controlled delay circuit illustrated in Figure 1. Shared signal buffers in the 8x8 neighborhood invert (A) and delay (B) the shutter pulse coming from the H-tree. The delay in B is dependent upon the control voltage which is adjustable over a voltage range spanning .5 and 1.7 V producing gate widths between 200 and 650 ps. A is thus the exposure start edge, and B is the exposure end edge. The A and B signals are combined in a NAND gate in each pixel to form the gate pulse for the desired exposure time. The amount of logic necessary to provide the inverters and gate delays to provide the A and B signals takes more area than a single pixel has available so the logic is distributed among the pixels in an 8x8 neighborhood. Pixels are assigned an H-tree buffer, delay buffers, an A signal buffer, or a B signal buffer. The signals are then distributed to the pixels in the neighborhood where the NAND gate generates the gate pulse.

On a sub-nanosecond timescale the time that it takes a gate trigger to propagate across a large format imaging sensor can be significant. Thus a repeating "H-tree" structure (Figure 2) is used to transport the gate trigger to each 8x8 neighborhood in the sensor. Although the H-Tree does not provide the shortest signal path to any given neighborhood, it ensures an equal path length for the gating signals so that all of the neighborhoods receive the trigger simultaneously with a minimum of skew.

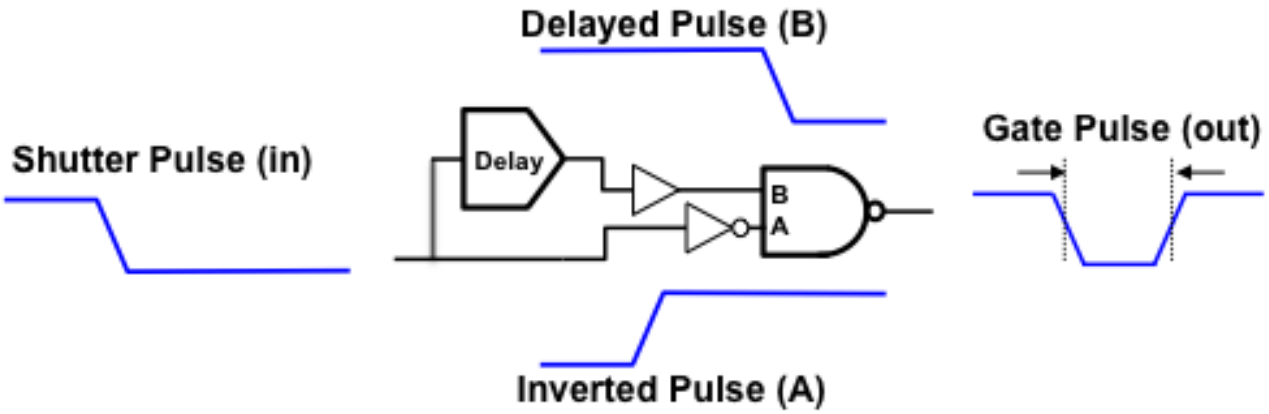

Figure 1. Logic circuit for local generation of exposure gate pulse

Figure 2. Image of part of a 64x64 array showing the H-tree structure for distributing the gate edge.

The 64 x64 test imager was fabricated using a 0.18 μm CMOS mixed-mode process. Pixels are 30 μm square and include the sampling circuit, the NAND gate pulse forming circuit, decoupling capacitors, readout circuitry and a photodiode detector. The photodiode enables the testing of the ROIC with visible light. The 64x64 sensor was designed as a self-contained test circuit; bump bond technology was to be developed as part of the follow-on program so bump landings were not included.

To further aid in evaluation the photodiodes in some of the pixels in each 8x8 neighborhood were sacrificed to accommodate test circuits that help to characterize skew, jitter, and dynamic range of the ROIC. Six pixels along the top and bottom edges of the neighborhood are tied to V_{dd} and ground to provide high and low signals, six pixels along the left edge have varying current sources, and the four corner pixels have circuitry for measuring the skew between adjacent neighborhoods. This leaves a 6x7 array of pixels in each neighborhood available for imaging. The pattern left by the test circuits and imaging pixels can be seen in Figure 3.

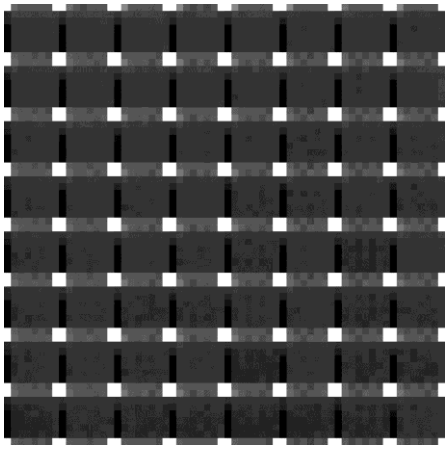

Figure 3. 64x64 image showing the test circuit and imaging pixels. The skew testing pixels are in white, the high and low pixels appear grey (arrayed horizontally between the skew pixels), and the current source pixels appear black (arrayed vertically between the skew pixels).

Optical tests of the 64x64 pixel prototype were performed using a 200 fs pulse width, frequency doubled (λ ~400 nm) Ti:Sapphire laser at the Short Pulse Laser Laboratory (SPL) at National Security Technologies LLC, Livermore Operations (NSTec-LO). The beam was formatted to underfill the ROIC and the Gaussian spatial profile of the beam can be seen in images (Figure 4).

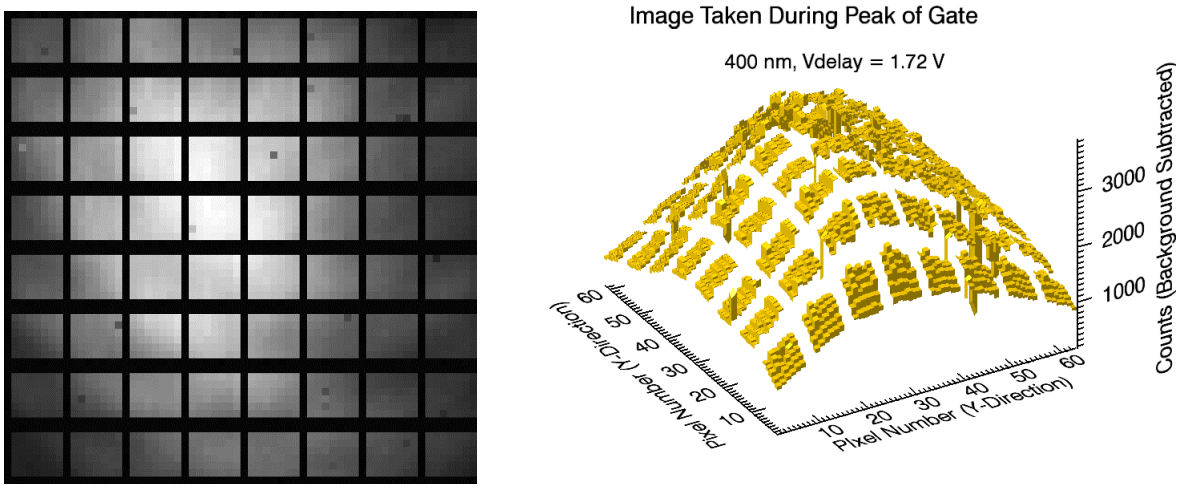

Figure 4. Left: Image of a 400 nm approximately Gaussian beam (t_{pulse} ~ 200 fs) illuminating the 64 x 64 image sensor with test circuitry pixels masked out. Right: 3-D image of a similar beam.

The SPL's timing system was used to vary the timing between the output 200 fs laser pulse and the gate trigger edge sent through the H-tree. By capturing images at varying times and plotting the average DN for the imaging pixels a temporal profile of the exposure gate (gate profile) is formed. The temporal duration of the gate is controlled by a user adjustable analog voltage V_{delay}. Two examples of this are shown in Figure 5. With the minimum setting of V_{delay} = .5 V the gate is ~200 ps long (left panel) at the maximum setting of V_{delay} = 1.7 V (right panel) the gate is ~650 ps long. The timing system used for these measurements had an RMS jitter of order 50 ps and dominates the observed scatter in DN values (at a nominal delay setting) observed on the rising and falling edged of the ~ 200 ps gate pulse.

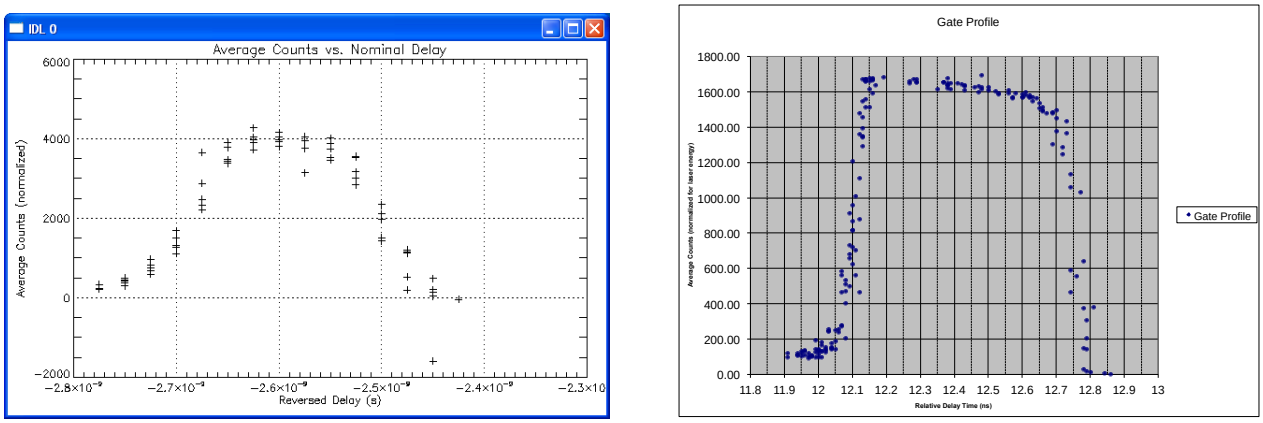

Figure 5. Left: Gate profile with V_{delay} set to 0.5 V resulting in a gate length of ~200 ps. Right: Gate profile with V_{delay} set to 1.7 V resulting in a gate length of ~650 ps.

These measurements validated the use of local gate generation in combination with the H-Tree trigger distribution to provide low-skew gating of large arrays.

III. 512 x 512 READOUT INTEGRATED CIRCUIT

The 512 × 512 ROIC also is a 30-µm pixel design. The repetitive nature of the H-tree structure readily allowed 8x scale-up in both dimensions to produce a 512x512 array. An added feature of this design, illustrated in Figure 6 is the ability to independently gate each of the four quadrants of the 512x512 readout. This is accomplished by the use of an AND gate to combine the common and independent shutter inputs at the major H-Tree of each quadrant. In this design the

ROIC responds to the negative going edge of a shutter signal. In common mode the individual quadrant shutter inputs are tied high and all quadrants trigger in response to the negative going edge of the common shutter input. Conversely quadrants are gated independently when the common shutter input is held high and a negative going edge is received at each quadrant shutter input.

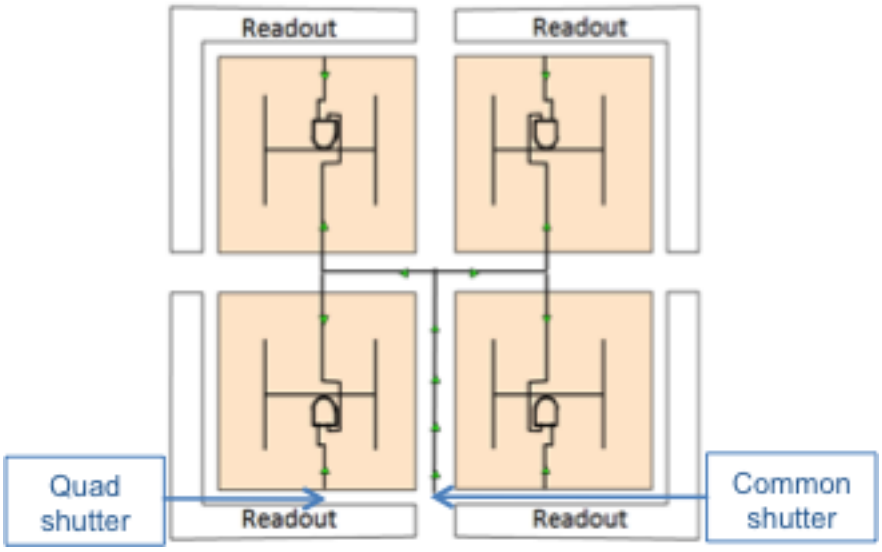

Figure 6. H-tree structure for 512 x 512 ROIC showing the common and individual quadrant shutters. The gap between quadrants in the figure is exaggerated and is not visible on the ROIC.

An optical micrograph of the sensor is shown in Figure 7. Unlike the 64 x 64 ROIC, the 512 x 512 ROIC is designed for bump-bonding of an X-ray sensitive photodiode array. Consequently the pixel design includes bump landings on the top level. A photodiode is included in the pixel design so unbumped sensors can still be tested and qualified, but the photodiode area is no more than 11% of the pixel area due to blockage by bump landings and, in certain pixels, H-tree metal.

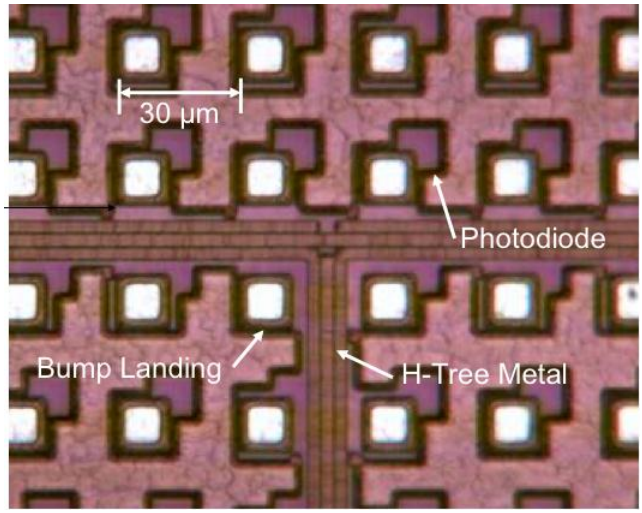

Figure 7. Microscopic view of the pixels showing the locations of bump landings, photodiodes, and H-tree metal.

The 512 x 512 ROIC has a much smaller number of pixels allocated to test circuitry. Sacrificed pixels include top and bottom rows of the array and 64 pixels distributed across each quadrant which provide a combination of high, low, and fixed current pixels(see Figure 8).

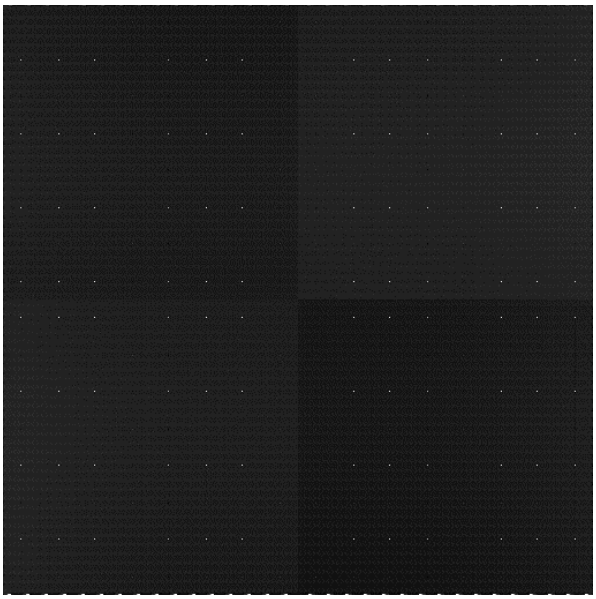

Figure 8. Background image of 512 x 512 ROIC showing test circuit pixels in the top and bottom rows and interspersed through the array. Difference in background levels is due to independent signal chain and analog-to-digital converters in the four quadrants.

The ROIC was mounted in a Kovar™ package that included a thermoelectric cooler (TEC) and is mounted on a sensor electronics board (shown face on in Figure 9 left). The board set for operation and readout is mounted behind the sensor board is obscured in this view. The prototype camera is operated via custom IDL® software on a computer communicating with the camera over a commercially-available Camera Link™ interface. In a typical Si imaging device near room temperature each 7 to 8° C of cooling reduces dark current in Si by a factor of two [6] so use of the TEC is desirable. However cooling the ROIC in room air would make it vulnerable to condensation and the board set was not designed to be run in a vacuum. Therefore the camera is housed in an airbox (Figure 8, right) that allows operation of the TEC and cooling of the ROIC to 0° C in a dry N_2 atmosphere. The airbox includes a port that may accommodate an optical bandpass filter or an X-ray window. The former is used for testing with UV lasers, while the latter is for future us once ROICs are bump bonded with X-ray sensitive photodiodes.

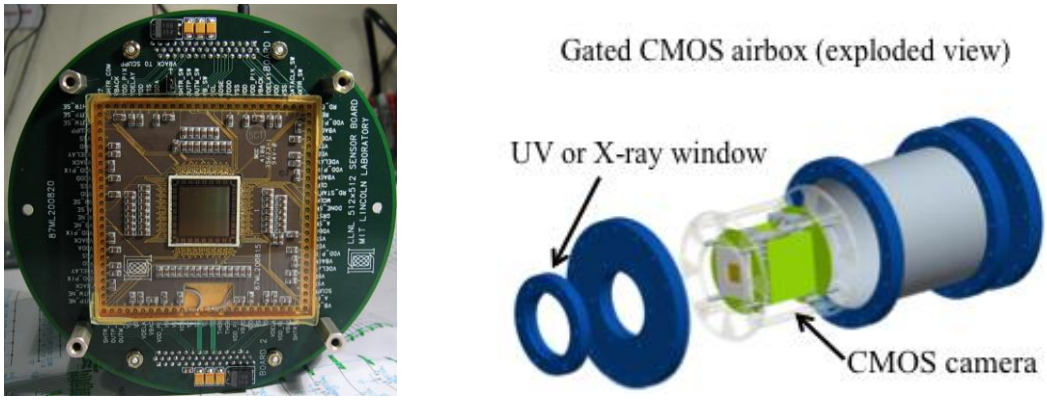

Figure 9. Left: ROIC (center) in Kovar package (gold) mounted on electronics sensor board. Right: Exploded view of airbox housing

Gate profile measurements were done at NSTec-LO at the newly commissioned Enhanced Short Pulse Laser laboratory (ESPL). In comparison to the SPL, the ESPL provides higher pulse energy and shorter (~ 50 fs) pulse length. The higher pulse energy ensured that the ROIC photodiodes could be saturated, but the fidelity of the temporal measurements was limited by jitter in the trigger system so no advantage accrued due to the short pulse length .

Again we employed a measurement wavelength of λ~ 400 nm. A narrowband optical laser-line filter on the airbox port eliminated stray light. The delay time between the shutter trigger pulse and the arrival of the laser pulse at the sensor was varied to measure gate profiles at the minimum and maximum values of V_{delay}.

The measured gate length at V_{delay} = .5 V is approximately 250 ps, while the gate length for the maximum V_{delay} = 1.7 V is approximately 2.7 ns (Figure 10). Each point in the plots is an average value for a subsection of the ROIC with 100 images taken at each time step. The amplitude variations on the rising and falling edges of the gate are indicative of the effects of jitter in either in the ESPL timing system or the ROIC/camera itself. The timing system in the ESPL has an RMS jitter of approximately 25 ps and contributes a significant portion of the jitter seen in the plots. Also, the amplitude variation along the peak of the gate pulses is higher than would be indicated by relative laser pulse energy measurements taken simultaneously with the images. Work is in progress to identify the sources of jitter and noise in the measurements to better quantify the performance of the ROIC and supporting electronics.

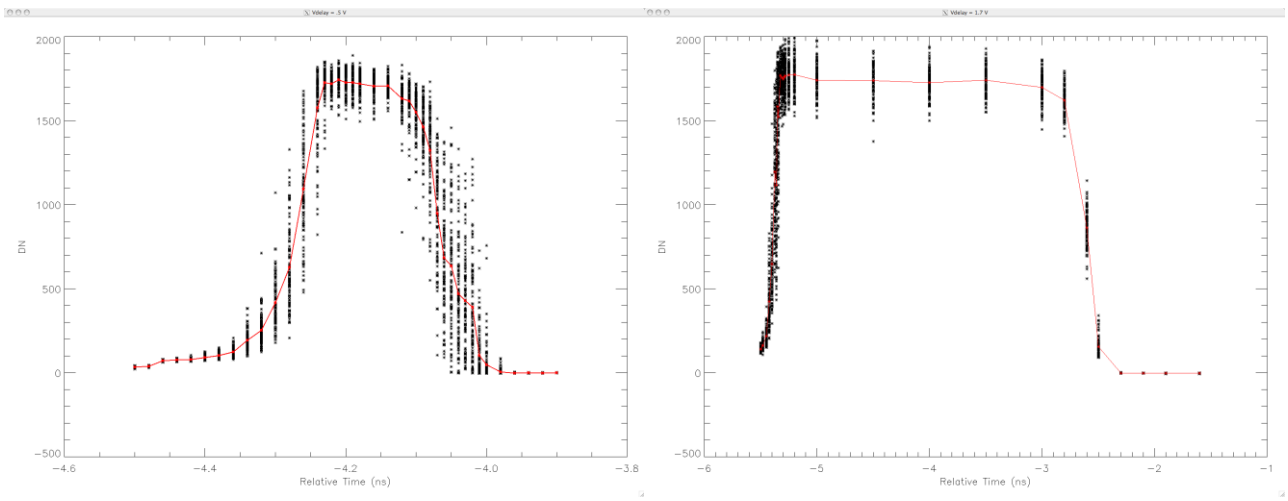

Figure 10. Left: Gate profile for V_{delay} = .5 V with FWHM of ~250 ps. Right: Gate profile for V_{delay} = 1.7 V with FWHM of ~2.7 ns.

Figure 11 shows a sequence of images acquired with the quadrants independently gated. A laser illuminated Air Force 1951 resolution target was imaged onto the ROIC with a simple lens system such that each quadrant of the ROIC contained part of the image. The camera was configured to accept triggers on the quad shutter inputs seen in Figure 6. In the sequence of Figure 11 the upper right quadrant was triggered first. Rotating counterclockwise each quadrant trigger is delayed by 100 ps relative to its predecessor. The laser was delayed relative to the upper right quadrant trigger in 50 ps increments. The sequence of twelve images corresponds to 550 ps of temporal delay between the first and last image.

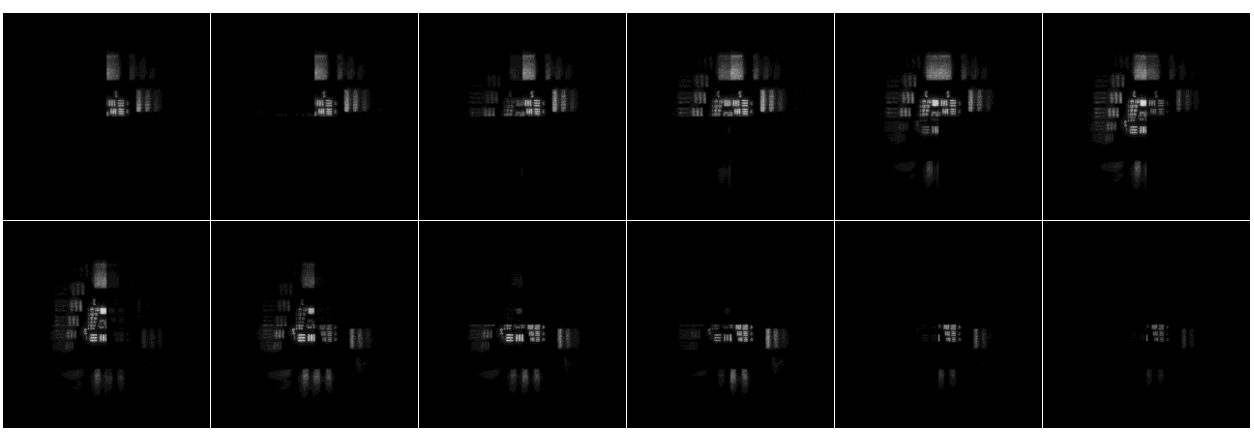

Figure 11. A sequence of images showing independent gating of the four quadrants of the 512 x 512 ROIC. Time increases from left to right and top to bottom in 50 ps steps.

IV. LOW ENERGY X-RAY SENSORS

Our preliminary design for the sensor is a back-illuminated, 20 μm thick Si photodiode biased at 20V. Assuming a Si saturated carrier velocity[7] of 10^7cm/sec, the detector can provide ~200 ps temporal response with good quantum efficiency for x-ray energies below 10 keV. The sensor is continuously active so a mechanism to dump the photocurrent before and after image acquisition is needed. Current return is provided by metal-filled, through-wafer vias that shunt the diode current when the ROIC sampling gates are closed. Images are acquired by diverting the sensor current to the ROIC sampling capacitors during the gate. This architecture requires that we sacrifice a small number of signal pixels in the sensor interior for current return and provide additional shunting vias at the wafer perimeter. The details of the sensor design will be presented in a forthcoming publication[8].

V. CONCLUSION

We have developed a general-purpose, gated CMOS read-out integrated circuit with a user selectable gate. An H-tree trigger distribution system supplies low-skew trigger signals to 8x8 pixel neighborhoods where local circuitry processes the input to generate the pixel gates. The gate width is voltage programmed and user selectable over a temporal range between 250 ps and 2.7 ns. Test of the trigger performance and measurement of the gate profile were performed with short pulse, frequency doubled Ti:sapphire laser radiation as an excitation source for on-chip photodiode sensors contained within each pixel. Ongoing experiments are improving the fidelity of the gate profile measurement and better quantifying the noise of the ROIC by improving uniformity of sensor illumination and limiting high spatial frequency amplitude noise in the laser output. We are actively pursuing development of x-ray photodiode arrays which will be bump-bonded to the ROIC to form a 512x512 element soft x-ray gated imager.

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