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Leakage current reduction via scallop-free Bosch process for high aspect ratio Si p-i-n diodes

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Smooth Bosch etch for improved Si diodes

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***Abstract*— A modified Bosch process is used to reduce leakage current resulting from surface damage and roughness for high aspect ratio pillars fabricated from Si p-i-n structures. C_4F_8 is used during both the etch and passivation steps in order to achieve a scallop-free and vertical structure. A 5x decrease in both the reverse bias leakage current and corresponding improvement in effective carrier density, charge density, depletion width, and minority carrier lifetime are observed using this process, indicating that surface charge states are decreased using this process. This can impact a number of three dimensional next generation devices.**

***Index Terms*— Silicon, etch, diode**

I. Introduction

MICRO- and nano-scale three dimensionally structured semiconductor devices have been under intense development for a number of applications during recent years. Applications include sensors[1,2], photovoltaics[3], betavoltaics[4], thermoelectrics[5,6], and catalysis[7]. Many of the devices utilize Si diodes. Because these structures have high surface-to-volume ratios, their performance can depend critically on the quality of the surface and the density of surface states. These states can act as recombination centers, increase leakage current, and increase capacitance, all of which potentially degrade device performance by increasing the electronic noise or reducing the signal collection. Passivation by dielectric coatings in some cases can remedy these issues [8,9], but imperfect coatings can introduce interface charge, increase capacitance, and decrease signal collection. For these reasons, an alternative approach may be desirable. Bottom up approaches for devices are being explored[5,6], but are generally limited to the nanoscale and lack geometric control. High aspect ratio structures can be fabricated using anisotropic wet etching using potassium hydroxide (KOH), isopropyl alcohol (IPA), and tetramethylammonium hydroxide (TMAH), the structures are limited by the crystallographic etch dependences for these etchants. Deep reactive ion etching (DRIE) remains a commonly used technique for creating these structures, particularly the Bosch process which utilizes a time multiplexed etch switching between etch and passivation cycles to produce highly vertical structures. Unfortunately, typical Bosch recipes produce a periodic scalloping due to this switching. This has been reported to be a source of localized strain when dielectric and metal coatings are introduced for through wafer vias.[10] In addition, the exposure of a semiconductor sidewall to the plasma can result in significant surface damage.[11-14] In this work, we describe a modified etch recipe which eliminates the scalloping and acts to reduce the density of surface states.

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II. EXPERIMENT

PIN Si diodes with a 24.2 μm intrinsic region were epitaxially grown by metal organic chemical vapor deposition (MOCVD) on an n-type Silicon substrate with doping density of 1 x 10^{18} cm^{-3}. An intrinsic region with n-type doping density of 2 x 10^{13} cm^{-3} was measured, resulting in a resistivity of >150 Ω-cm. A 0.8 μm p+ region (1 x 10^{19} cm^{-3}) was grown on top of the 24.2 μm i-region. Wafers were patterned using standard photolithography with nLOF 2035 negative photoresist (PR), with a mask thickness of 2.8 μm. The pattern consisted of 2 μm x 2 μm circular pillars arrayed in a square matrix with a 4 μm pitch. The wafers were cleaved into 1 cm x 1 cm square samples and etched in a Surface Technology Systems Bosch etcher using recipes summarized in Table I.

TABLE I
ETCH RECIPE PARAMETERS FOR STANDARD AND SMOOTH BOSCH ETCHES

	Standard recipe	Modified recipe
Source power	600 W	600 W
Platen power	12 W	12 W
Passivation gas	80 sccm C_4F_8	10 sccm C_4F_8
Passivation time	9 s	10 s
Etch gas	25 sccm SF_6	25 sccm SF_6
		50 sccm C_4F_8
		Vary 0-25 sccm O_2
Etch time	12 s	12 s
Pressure	15 mTorr	15 mTorr

A standard Bosch process was compared with a modified process incorporating C_4F_8 passivation during the etch step as well as varying amount of O_2 intended to increase the etch rate. After etching, the photoresist and any remaining sidewall polymer was stripped in solvent. Scanning electron microscopy (SEM) was used to examine the verticality and sidewall morphology of the etched samples. A previously described planarization process[15] was used prior to depositing Al/Cr/Au (500/50/750 nm) electrodes on the top

and bottom of the structure. Electrical characterization was performed on selected samples in the form of current-voltage (IV) and capacitance-voltage (CV) using a Keithly 4200. Open circuit voltage decay (OCVD) using a circuit and method described by Bellone and Licciardo was used to extract carrier lfietime.[16]

III. RESULTS

Table II describes the etch rates observed for Si and photoresist for the recipes examined. The smoothest recipe contains no O_2 during the etch step, but also possesses both the lowest Si etch rate and the lowest Si:PR selectivity. A positive taper of 0.5^o from top to bottom of the pillar was achieved along with no visible scalloping up to a magnification of 20,000x. As O_2 is added, the Si etch rate increases, resulting in increased scalloping due to a change in the balance between the deposition and etch rates during the etch step. Fig. 1a shows micrographs of etches with our standard Bosch process and with the smoothest modified recipe. For the Smooth etch, an image has been chosen with an imperfect photoresist profile which results in damage to the top of the Si as the mask is eroded. The etch rate is highly dependent on the time chosen to etch, declining during etching. Although this recipe is more limited in height than the standard recipe, which can achieve >50 µm structures, heights of 20-30 µm have been achieved.

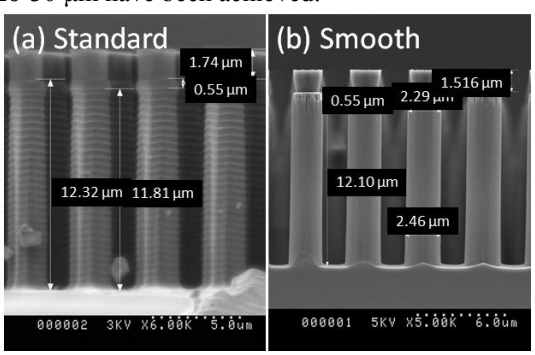

Fig. 1. Standard and smooth (0 O_2) profiles

TABLE II
SUMMARY OF ETCH RATES, SELECTIVITY, AND OBSERVED SIDEWALL ROUGHNESS FOR VARIOUS RECIPES

Recipe	Si ER (µm/min)	PR ER (µm/min)	Si:PR	Comments
Standard recipe	1.11	.05	22:1	Severe scallops
Smooth with 0 sccm O_2	0.18	.018	10:1	Smooth
Smooth with 5 sccm O_2	0.30	.018	16:1	Very faint scallops
Smooth with 10 sccm O_2	0.42	.016	26:1	Faint scallops
Smooth with 15 sccm O_2	0.47	.014	33:1	Small scallops
Smooth with 20 sccm O_2	0.56	.01	56:1	Small scallops, negative taper
Smooth with 25 sccm O_2	0.58	.0074	78:1	Small scallops, negative taper

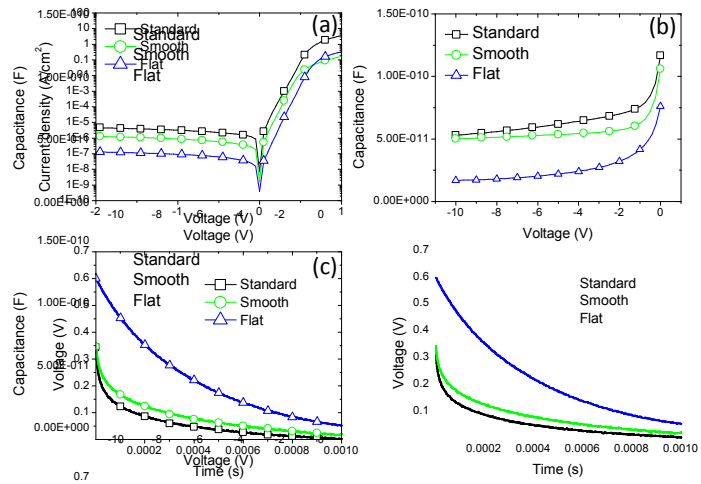

Fig. 2. (a) Current-voltage (b) capacitance-voltage and (c) open circuit voltage decay characteristics for tested diodes

For electrical testing, the recipe with no O_2 was chosen because it gave the smoothest sidewall. The effects of native oxide passivation are not considered, as it is expected to affect each device equally. Fig. 2 shows (a) the current-voltage (b) the capacitance-voltage and (c) the open circuit voltage decay characteristics of the diodes fabricated. Diodes have been fabricated on unetched, flat material for comparison. In Fig. 2a, differences are observed in both forward and reverse bias. In reverse bias, the Smooth recipe results in leakage current that is an order of magnitude less than using the Standard recipe. Reverse bias current is governed by the equation

$$J_{rev} = \left(\frac{qD_h}{L_h N_D} + \frac{qD_e}{L_e N_a}\right) n_i^2 + \frac{qwn_i}{\tau_g} \qquad (1)$$

The former term describes diffusion current and the latter generation current. D is the diffusivity of carriers, L is the diffusion length of carriers, q is the electronic charge, n_i is the intrinsic carrier concentration, w is the depletion width, and τ_g is the generation-recombination lifetime. The increased current in reverse bias for the Standard etch is attributed to increased generation due to surface damage. Using the intrinsic region doping value of 2 x 10^{13} cm^{-3} as the baseline for the Flat diode, the effective free carrier density of the intrinsic region for the Standard and Smooth etch diodes were extracted from the ratios of J_{rev} and are shown along with other extracted parameters in Table III. The forward current of a diode is described by

$$J = J_0 exp\left(\frac{qV}{\eta kT}\right) \qquad (2)$$

η is the ideality factor. η of 1 indicates recombination limited by the minority carrier, while a value of 2 indicates that it is limited by both carrier types and is a result of increased defect recombination. In this case, the ideality factor is between 1 and 2 and the diodes display both types of recombination. The Flat and Smooth etch samples show similar ideality factors while the Standard etch shows a larger one.

TABLE III
EXTRACTED DIODE PROPERTIES

	Effective carrier density	Ideality factor	Built in voltage at	x_d at 0V at p-i	Charge density (cm^{-3})	τ_{p0} (µs)

	(cm^{-3})		p-i (V)	(μm)		
Flat diode	$2.1x10^{13}$	1.6	0.73	6.7	$2.1x10^{13}$	36
Std etch	$1.7x10^{15}$	1.9	0.49	0.89	$8.1x10^{14}$	<3
Smooth w/ 0 sccm O_2	$3.6x10^{14}$	1.6	0.44	0.98	$5.9x10^{14}$	6

The capacitance-voltage characteristics shown in Fig. 2b also indicate increased charge density for the Standard compared to the Smooth etch, which are both increased compared to the Flat diode. Extracted values are shown in Table III. The built in voltage (V_{bi}) and depletion width (x_d) are given for the p-i interface. This is because the height of the pillars is not sufficient to expose the n-i interface to the plasma. V_{bi} can be extracted from the x-intercept of a plot of $1/C^2$ vs V while the effective charge density can be extracted from the slope using the equation

$$N_D = -\frac{2}{q\epsilon_s}\frac{1}{\frac{d(\frac{1}{C^2})}{dV_a}} \quad (3)$$

The effective charge density is observed to be greater than the effective free carrier density; this is attributed to the fact that the plasma damage creates charged defects along the surface which are located within the band gap. These are observed using the CV extraction, while only the free carrier density is observed using the JV extraction. The increased surface charge of the etched diodes increases the voltage required to achieve full depletion of the i-region. At 0V, the depletion width x_d is given using the one sided junction approximation,

$$x_d = \sqrt{\frac{2\epsilon_s}{qN_D}(V_{bi})} \quad (4)$$

N_D is the previously extracted charge density in the intrinsic region. An increased charge density on the sidewall increases the effective number of dopants in the lightly doped intrinsic region while not appreciably changing the number of charge carriers in the highly doped p+ region. This results in x_d decreasing at 0V and requires a higher reverse bias voltage to fully deplete the device.

Effective carrier lifetime was monitored by open circuit voltage decay, Fig. 2c. Values are shown in Table III. In this method, a diode is forward biased to achieve a steady-state excess carrier concentration in a lightly doped region. Subsequently the diode bias is removed to enable recombination of the excess carriers. At low level injection, the minority carrier lifetime (τ_{min}) can be extracted by plotting the function F(t) given by

$$F(t) = \left[-\frac{q}{\eta kT}\cdot\frac{dV_D(t)}{dt}\right]^{-1} \quad (5)$$

τ_{min}, in our case τ_{p0} for holes, is given by the local minimum of the F(t) curve.[16] k is Boltzmann's constant, T is the temperature, η is the injection dependent ideality factor, and V_D is the measured voltage. Extracted lifetimes are shown in Table III. Both the Standard and Smooth etch have lower lifetimes than the Flat diode. The Smooth etch shows an improvement of at least 2x over the standard etch.

IV. Conclusion

We have developed an improved Bosch etch recipe which produces smooth, scallop free sidewalls. Using an etch that incorporates C_4F_8 into the etch step results in superior profiles with improved electric characteristics compared to a typical Bosch etch. This is attributed to a decrease in surface states and damage.

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