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# Mk x Nk gated CMOS imager

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## ABSTRACT

Our paper will describe a recently designed Mk x Nk x 10 um pixel CMOS gated imager intended to be first employed at the LLNL National Ignition Facility (NIF). Fabrication involves stitching MxN 1024x1024x10 um pixel blocks together into a monolithic imager (where M = 1, 2, . . . 10 and N = 1, 2, . . . 10). The imager has been designed for either NMOS or PMOS pixel fabrication using a base 0.18 um/3.3V CMOS process. Details behind the design are discussed with emphasis on a custom global reset feature which erases the imager of unwanted charge in ~1 us during the fusion ignition process followed by an exposure to obtain useful data. Performance data generated by prototype imagers designed similar to the Mk x Nk sensor is presented.

**Keywords:** CMOS and CCD scientific imagers.

## I. INTRODUCTION

The National Ignition Facility (NIF) is a 192 beam frequency tripled Nd-glass laser system designed to deliver a highly shaped 1.8 MJ beam into a hydrogen fuel target within ~ 21 ns to produce nuclear fusion ignition.<sup>1</sup> Streak<sup>2</sup> and framing<sup>3</sup> cameras located within the 10 m diameter target chamber provide spatial and time resolved images of the inertial confinement fusion implosions. X-rays from the implosion are converted to electrons inside each camera which in turn are converted to visible light with a phosphor screen. A fiber optic faceplate couples the phosphor screen to a Kodak 16801E 4k x 4k x 9 um pixel CCD. From there signal charge is integrated and readout by the camera system.

During and after implosion the CCD is exposed to large doses of high energy radiation resulting in two primary problems for the imager: 1) permanent ionization / bulk damage to the point where a camera must be replaced and 2) unwanted background charge generation during implosion which must be erased before an image can be taken. These issues can be significantly relaxed by using a CMOS imager instead of a CCD. For example, CMOS pixels in general are more radiation tolerant given that they can be directly read using random access addressing. This feature preserves charge transfer efficiency (CTE) since only one transfer within the pixel is required. In comparison a 4k x 4k CCD must perform thousands of transfers to move charge to the output amplifier making the device vulnerable to bulk state traps that rapidly degrade CTE with the dose level. Also CMOS exhibits very little flat-band shift caused by ionizing radiation (i.e., fixed charge build up in the oxide layer). This is because the gate oxide for CMOS is considerably thinner (~50A) than the CCD (~2000 A) in addition to typically better SiO<sub>2</sub> quality to prevent flat-band shift. Excessive flat-band shift plays havoc on operating voltage settings to the point where the imager just stops working. Multiphase CCDs may begin to show signs of flat-band shift at few tens of krds. In contrast CMOS can handle levels greater than 1 Mrd.<sup>4</sup>

The background charge difficulty is primarily generated when 14 MeV neutrons interact with the target chamber walls and diagnostic housing. The reaction produces secondary protons, alpha particles, and gamma radiation. Most of this radiation passes after ~ 1 us leaving a CCD saturated with charge (refer to Fig 1). It is very important to the application that an image be quickly captured after erasure before the phosphor image signal intensity decays away. Unfortunately

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the CCD must be fully read before an exposure can be taken which takes time. In contrast, a CMOS sensor can be erased in very short order ( $\sim 1$  us) by a custom gated 'global reset' feature discussed below.

The basic format structure for the  $M_k \times N_k \times 10$  um pixel imager is shown in Fig. 2a. The user selects the size of the imager to be fabricated by choosing  $M$  and  $N$  where  $M = 1, 2, \dots, 10$  and  $N = 1, 2, \dots, 10$ . For example, a 10k x 10k imager can be fabricated by selecting  $M=N=10$ . The illustration shows a 4k x 4k imager comprised of sixteen individual 1k x 1k blocks ( $M=N=4$ ). Each block is read in a serial or parallel fashion by activating the horizontal and vertical enables shown (e.g., EX1, EY1). Figure 2b shows the four individual patterns contained within the reticule that are 'stitched' together on a 200 mm silicon wafer to produce the monolithic imager. For example, Fig. 3 shows a wafer map that produces nine 4k x 4k imagers in addition to several 1k x 1k smaller imagers. It is possible to mix different format imagers on a given wafer (e.g., 4k x 4k, 2k x 2k, 1k x 1k).

The  $M_k \times N_k$  imager is designed to be fabricated at TowerJazz Semiconductor using their base NMOS or PMOS 0.18 um 3.3 V / 5 V processes. The numerous custom pixel implants used are usually varied by changing dose and energy to best fit the application and performance desired. LLNL has elected to fabricate a frontside illuminated (FSI) 4k x 4k imager (backside illumination (BSI) is left as an option for later). Standard Jazz silicon (boron, 20 ohm-cm, 9 um epi thickness) will be employed (custom silicon is also an option for the customer if desired). The imager design is complete and ready for fabrication.

Figure 4 presents a block diagram of a 2k x 2k imager showing six major components; 1) pixels, 2) pixel drivers, 3) row X address decoder, 4) column Y address decoder, 5) column correlated double sampler (CDS) processor and 6) column select multiplexer and output buffers. Discussions in this paper assume NMOS processing will be employed where electrons are collected and transferred (as opposed to holes) although the  $M_k \times N_k$  can also be fabricated using PMOS technology depending on the performance need. Switching the design from NMOS to PMOS or vice versa involves one reticule. Disadvantages and advantages between PMOS and NMOS technologies are discussed in Ref. 4.

## II. $M_k \times N_k$ GENERAL LAYOUT AND FEATURES

### 2.1 Pixels

Pixels are fabricated using the reticule pattern shown in Fig. 2b. Figure 5 shows a cross-section of a single 5T pinned photo diode (PPD) 10 um pixel employed by the  $M_k \times N_k$  imager. A read cycle of the pixel typically begins with resetting of the sense node (SN) to the reference potential  $V_{REF}$  through application of a simultaneous clock pulse to both gates of the reset and the metal-insulator-metal (MIM) select MOSFETs. After the sense node is reset, either the *MIM\_clk* (if in the high gain mode) or *reset\_clk* (if in the low gain mode) is removed allowing the SN to settle to its final reset voltage. The PPD region of the pixel collects photo electrons generated by the underlying silicon for a given integration/read time. The electrons are transferred to the SN by clocking the transfer gate (TG) clearing the PPD region preparing the next integration cycle. The source follower (SF) buffers the video that is applied to the column video bus when the row select MOSFET is activated (via *row\_clk*). From there the column bus goes to the CDS (refer to Sec. 2.5). The SF current is adjusted by the user (via *pixel\_I*) for the amount of current critically determines the dynamic range and power consumption of the pixel.

### 2.2 Pixel drivers

The pixel drivers are included in the 'left' reticule pattern shown in Fig. 2b. There are four pixel bi-polar drivers contained in each row of the device that drive the reset, row select, TG and MIM gates of the pixel. The clock drivers switch between high and low voltages set externally by the user for optimum performance. Adjustment is best done by viewing the raw pixel video with an oscilloscope (refer to Sec. 2.5 below). Charge capacity, dynamic range, CTE, speed, linearity, dark current etc. are all influenced by the pixel operating voltages. The clocks input to the drivers are externally controlled by the user for timing also plays an important role in the optimization process.

### 2.3 Row X address decoder

The row X address decoder is also found in the 'left' reticule pattern of Fig. 2b. The rows of the  $M_k \times N_k$  imager are divided into  $N$  blocks of 1024 rows each. The vertical *Y\_enable\_clks* select the blocks to be read. Rows within each block are addressed by 10-bits of *Y\_add\_clks* decoded for values from 0 (row closest to pixel 1,1) to 1023. The row addresses are captured on the rising edge of the *Y\_latch\_clk* provided. The row address only activates the pixel drivers

for the row being addressed. Clocks for other rows are held low (except for the reset which can be controlled with the *reset\_MIM\_clk\_N*). The X-Y addresses are externally controlled by the user of the device.

#### 2.4 Column Y address decoder

The column Y address decoder is also located in the 'bottom' reticule pattern of Fig. 2b. The columns of the imager are divided into M major blocks of 1024 columns each. The horizontal *X\_enable\_clks* selects the blocks to be read. The blocks are further divided into four sub arrays (s4 . . . s1) of 256 columns. They are enabled with the 2-bit *output\_mux\_enable\_clks*. The columns within each sub array are addressed by 8 bits of *X\_add\_clks* decoded for values from 0 (row closest to pixel [1,1]) to 255. The column addresses are captured on a rising edge of the *Y\_latch\_clk*. The M blocks can be addressed a block at time or activated in parallel for high speed readout. The CDS outputs can be further muxed so that all M blocks can be read with a single output (*muxed output*) located in the lower left hand corner (i.e., the 'corner' reticule pattern in Fig. 2b).

#### 2.5 Column correlated double sampler (CDS) processor

The CDS processor is located in the 'bottom' reticule pattern of Fig. 2b. When a row is selected the pixel output is directed into the column's CDS block shown in Fig. 6. At its input a RC filter is found with time constant  $\tau_D$  (built into the circuit at  $\sim 5$  us). The resistive component can be activated with the *BW\_clk* to lower noise before entering the CDS processor. Next we encounter the *raw\_enable\_clk* switch which allows the customer to either examine the raw pixel video or utilize the on-chip CDS circuitry. Having access to the raw channel is essential to adjusting pixel voltages and clock timing for optimum performance (in the same fashion to how CCD pixels are set up). The raw channel is also required for off chip digital (dCDS) processing used for global shutter (SNAP) readout.

When *raw\_enable\_clk* is activated the pixel video is directed into the CDS circuit. CDS processing takes place by first resetting the pixel ( $\sim 1$  us). At the same time the clamp switch is turned on for approximately  $5\tau_D$  sec (this assures that 'reset remnant noise' is insignificant to the SF read noise floor). During this time the video is clamped to a voltage set by *clamp\_offset*. This bias control usually sets the final DC offset zero signal level into the ADC under dark conditions. Shortly after the *clamp\_clk* is released the *TG\_clock* is switched high for a time period of  $\sim 1$  us. On the falling edge of the TG clock the *sample\_clk* is issued and left on for  $\sim 3\tau_D$  sec and then turned off to 'hold' the video signal. As shown in Fig. 6 the video can be held by one of two available sample capacitors. If the sampling of the next row begins before readout of the previous row is complete, the sampling can be directed to the second sample capacitor without interfering with the previous row's stored value (i.e., "ping-pong" operation). This method of sampling eliminates CDS overhead time when reading a row. Frame time will be essentially determined by either how fast the ADC can encode a row of pixels or limited by the buffer sample SF bandwidth.

The *clamp\_I* and *sample\_I* current adjusts determine the operating range and bandwidth of the clamp and sample SFs. If CDS processing is not being used the clamp and pixel SFs can be disabled using the *sample\_select\_clk* and *pixel\_row\_select\_clk* clocks. The sample SF must be left on while the ADC encodes the values held. However, disabling these SFs during a long integration period will significantly reduce on-chip power dissipation while eliminating possible sources of extraneous dark signal through transistor luminescence. During the integration period which precedes readout all three SFs can be disabled reducing power consumption to a negligible level.

#### 2.6 Column select multiplexer and output buffers

The column select multiplexer and the output buffers are also located in the 'bottom' reticule pattern of Fig. 2b. When *raw\_enable\_clk* is set high or low respectively, the four *CDS\_video* and four *raw\_video* signals for each 1k x 1k block are multiplexed to separate SF output buffers. Further, if the *single\_output\_clk* is set high these videos are muxed and directed to a single SF buffer located in the lower left hand corner of the imager for serial block readout (i.e., read one at a time). The *raw\_video\_output* pins are buffered by NMOS SFs whereas PMOS SFs are used for the *CDS\_video\_output* pins (these polarities are switched if PMOS pixels are fabricated). The transistors are sized to be able to drive the video signal off-chip at the pixel rates up to 15 Mpix/sec with a 10 pF load.<sup>4</sup> The PMOS outputs require external pull-up resistors to the *DIG\_VDD* supply while the NMOS outputs require pull-down resistors to ground. The net video time constant at the output of the imager is usually dependent on the load resistance and related load capacitance. However, the sample and hold SF may limit frequency response for very high speed operation. The current through the SF must be carefully adjusted by the user.

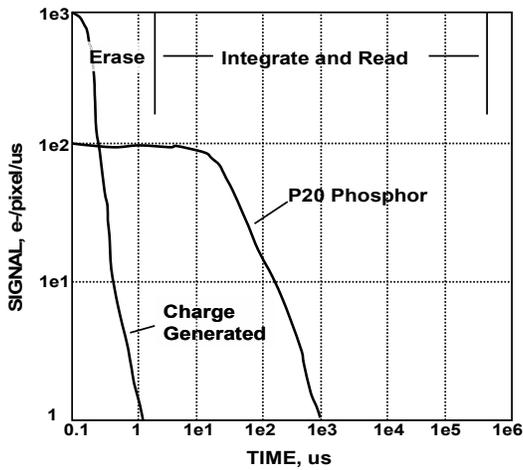
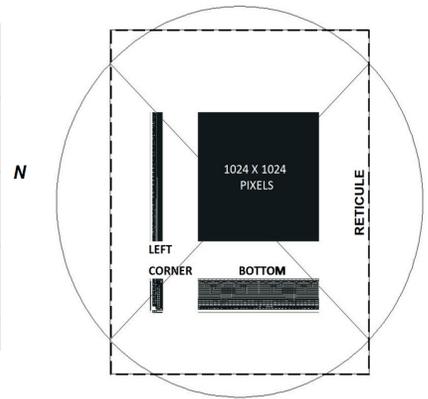
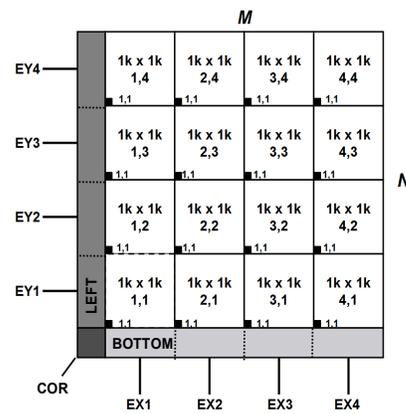


Fig. 1. Erase, integrate and read periods after implosion.



Figs. 2a,b. The  $M_k \times N_k$  imager and reticule patterns for stitching.

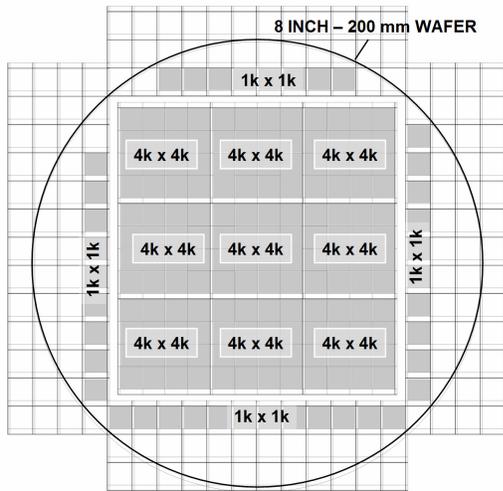


Fig. 3. 4k x 4k and 1k x 1k wafer map.

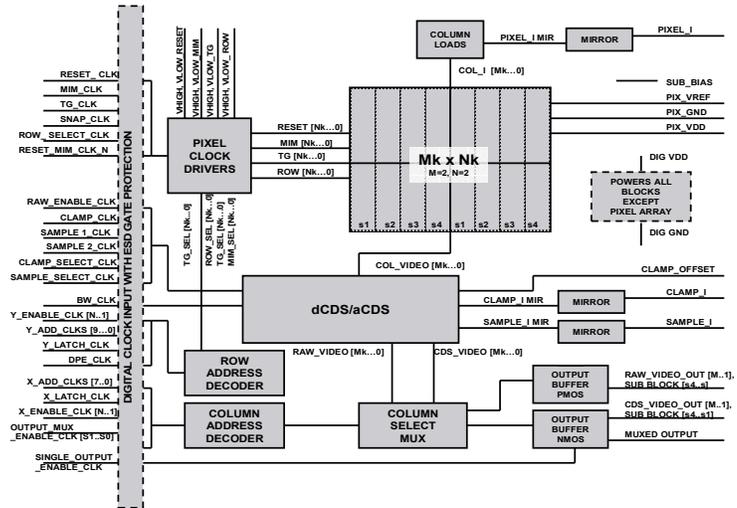


Fig. 4.  $M_k \times N_k$  functional block diagram.

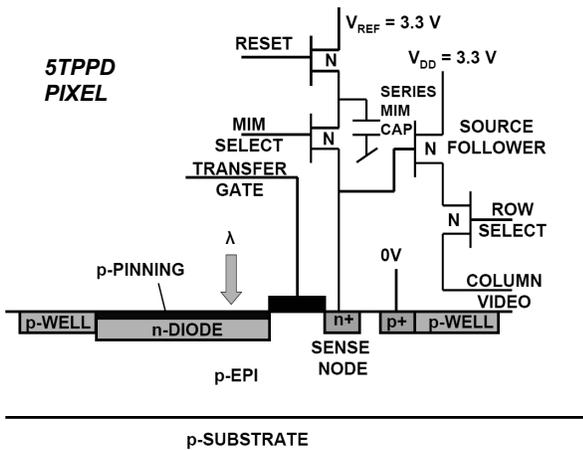


Fig. 5. The  $M_k \times N_k$  10 um 5TPPD pixel.

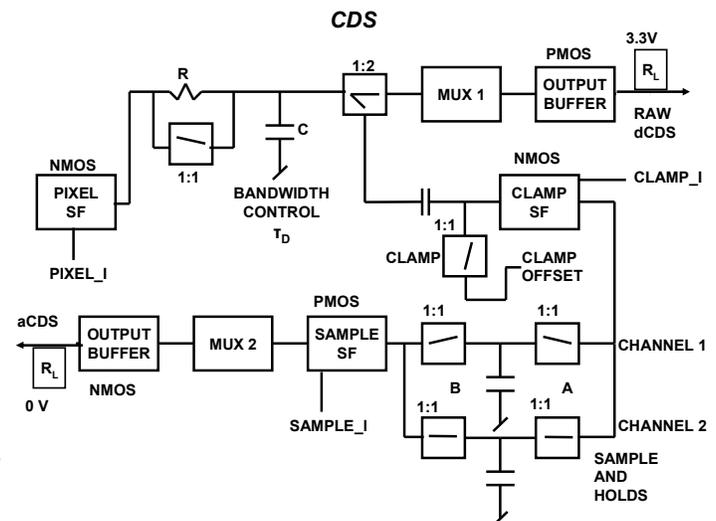


Fig. 6.  $M_k \times N_k$  column CDS processor.

## 2.7 Global shutter (SNAP) readout

Several different read modes and timing diagrams can be implemented by using the global shutter feature. One basic example is discussed here where minimum read noise is achieved using the *raw\_video\_output* dCDS channel. We start by applying global erasure discussed in Sec. 3 below. This operation is followed by progressively reading the raw reset values of each pixel off-chip. The reset levels are digitized and stored into a computer as a 'reset frame.' As reset levels are being read, signal charge collects in the PPD region of the pixels forming an image. After all reset levels are stored the *TG\_clk* and *SNAP\_clk* are globally applied to transfer signal charge from the PPD to the SN. The image on the SN is then progressively read off-chip. The video levels are digitized and stored into the computer as the 'signal frame.' The reset and signal frames are then subtracted pixel by pixel to produce the final image. This global read scheme will produce a read noise floor approximately equal to non global progressive readout using on-chip CDS processing (assuming dark current noise is negligible). The next frame will repeat the steps above beginning with global erasure. Since the pixels are reset at the same time, integrate over the same time interval and are transferred to the SN at the same time any motion artifacts are reduced to a minimum.

## 2.8 Miscellaneous features

The  $M_k \times N_k$  imager has ESD protection back-to-back diodes on the bond pads with MOSFET gate inputs i.e., the clocks on the left hand side of Fig. 4. Pads with diffusion inputs do not need protection. i.e., those voltages and outputs on the right hand side of Fig. 4. The absence of diodes allows pixel operating voltages to be greater than  $DIG\_VDD$  and less than *sub\_bias* (e.g., required for TG accumulation or inversion). The imager also includes eight rows of opaque pixels at the bottom of imager (contained in the bottom reticule pattern shown in Fig. 2b). These rows are independently addressed by activating *DPE\_clk* and using the first three *Y\_ADD\_clks*. The dark rows are important to remove remnant column to column CDS offset fixed pattern noise (FPN). The  $M_k \times N_k$  can be configured as a mosaic using two free sides of the device (top and right sides). Similar mosaicing has already been demonstrated for NASA's flight SoloHi 1920(V) x 2048(H) x 10 um 5TPPD pixel imager shown in Fig. 13).<sup>6,7</sup> The gap between devices can be kept to < 100 um depending on how accurately the wafer is sawed. Mosaicing must be considered for imagers larger than 4k x 4k because device yield is rather low above this size. For example, greater yield can be obtained when four 4k x 4k imagers are mosaiced together compared to a monolithic 8k x 8k device. There are two thinning options for the  $M_k \times N_k$  imager. If mosaicing is not desirable dummy bond pads on the top and right side of the imager are provided to make the thinning process more straight forward. Removing these pads for mosaicing significantly increases the thinning effort and related cost. Exposure can be controlled by erasing (via *TG\_clk*, *reset\_clk*) a row of pixels K rows behind the row being interrogated as progressive scan proceeds (i.e., rolling shutter). This way the integration period for the imager is determined by the difference in row counts multiplied by the time it takes to read and encode a row of pixels. Minimum exposure is when the row being erased is next to the row being read (i.e., K= 1). The exposure time, E, in equation form is given by  $E=1024KT_RN$  where  $T_R$  is the row read time (sec) and N is the number of vertical 1k blocks.

## 3.0 HIGH SPEED ERASURE

Global erasure entails quickly transferring unwanted charge to the  $V_{REF}$  drain found in all pixels. This can be readily accomplished by simply simultaneously activating *TG\_clk*, *reset\_clk* and *SNAP\_clk*. However, to achieve minimum erase time several design and fabrication requirements must be considered. For example, the  $M_k \times N_k$  can be a sizeable array and therefore it is important that clock pulses make their way to the furthest pixels from the pixel drivers with fast enough rise and fall times (located on the left hand of the device). The TG driver is the most critical since it has the largest capacitance to drive. For this reason the TG is double bused with extra wide metal to reduce buss resistance (~ 0.8 ohms/pixel). SPICE modeling and calculations show that erase time will be < 500 ns for the furthest pixel assuming a 4k x 4k imager. This design is reasonable to go with in that transfer speed will likely be dominated by PPD to SN transfer speed within the pixel as discussed below.

The energy and dose of the PPD implants (diode and pinning) must be carefully adjusted to produce a low PPD potential while having sufficient charge capacity. A 5 % difference in dose or energy makes a significant difference in how the pixel responds to erasure as well as overall performance. As practiced in the past, the  $M_k \times N_k$  imager will adjust the implants to produce a 2.3 V difference between the PPD and SN regions. Doing so generates a sizeable fringing field between the two regions required for fast transfer. The high field also curtails the amount of trapping that takes place in surface states located under the TG but not entirely. Hence, after the pixels are erased of charge the TG is clocked negatively into accumulation or inversion in the case of a buried TG (we will assume inversion for the sensors

characterized below). With inversion remnant trapped charge recombines with holes preventing it to escape back into the PPD as image lag (as discussed and demonstrated in Sec. 4. In addition to the trapping the problem the presence of a small thermal barrier at the front edge of the TG exists slowing down transfer time. The barrier problem can be managed by self aligning the PPD implants to the TG front edge. Also the large PPD to SN potential difference mentioned above reduces any remnant TG barrier that is left but not completely. Therefore, speed is rarely achieved as theory predicts because of the front edge TG barrier.

To give some feeling for the theoretical speed limit Fig. 7a plots PISCES modeling of the linear e-/um signal density,  $Q(t)$ , for a 32 um linear region as a function of transfer time assuming the four linear densities labeled in the plots. For example, at zero time a linear region of the 32 um pixel will contain  $1.6e5$  e- for a charge density of  $4.9e3$  e-/um (32 x 4900). Using these values, Fig. 7b plots charge transfer inefficiency (CTI) as a function of transfer time. For instance, the charge remaining after 20 ns is  $3.00e4$  e-. The ratio of  $3.00e4$  to  $1.6e5$  yields a CTI of approximately 0.2 (refer to the small circle in the plot). Note as the charge density increases CTI performance improves because of self induced drift. Figure 8a and 8b plot e-/um and CTI with transfer time for a family of pixel sizes assuming a density of  $4.9$  e-/um<sup>2</sup>. Transfer time increases by the square of the size as diffusion theory predicts.

Given the theoretical curves above and assuming a CTE of 0.999 is desirable, the transfer time for a 16 um pixel is ~ 200 ns assuming that 7840 e- is transferred (the Mk x Nk x 10 um pixel would be ~ 4x faster). Figure 9a shows experimental speed data for the 16 um pixel as the TG clock width is time varied. The plot shows that a TG clock width of ~ 1 us will satisfactorily erase the imager although slower than the 200 ns predicted by theory. The discrepancy usually implies that a small potential barrier at the front edge of the TG exists. Figure 9b shows some CTE speed improvement as the TG amplitude is elevated for a fixed TG clock width of ~ 100 ns. To examine the possibility of a TG barrier further Fig. 10 presents PISCES modeling results of the pixel showing in fact the presence of a small barrier when TG =1 V. Increasing the TG clock voltage pulls down and eliminates the barrier. Figure 11 plots CTI with transfer time assuming a 10 um pixel. A CTE of 0.999 is achieved for a transfer time of 100 ns assuming TG =1.25 V.

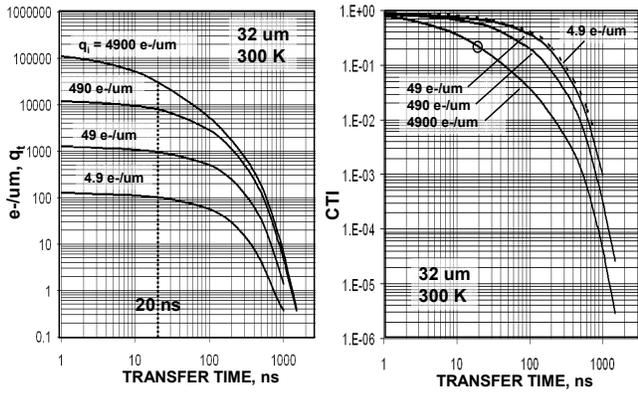
It should also be mentioned that residual bulk image (RBI) is often a problem when an imager is exposed to near IR light.<sup>5</sup> The photo electrons produced become trapped at the silicon's epitaxial interface. The charge from bulk traps is released as a dark current at a rate dependent on operating temperature. BSI imagers do not exhibit RBI since the epi interface is removed by the thinning process. Figure 12 shows residual images after a FSI 1024 x 1024 x 16 um 6TPPD pixel sensor (BIG MIN III<sup>4</sup>) is over exposed with 470 nm and 950 nm light in the center of the imager. The imager was globally erased immediately after the light source is turned off. The noninverted 470 nm response shows trapped charge under the TG whereas the inverted image does not for reasons explained above (i.e., hole recombination). The non inverted 950 nm images show both RBI and TG trapped charge whereas the inverted image is composed of only RBI.

## 4.0 PERFORMANCE

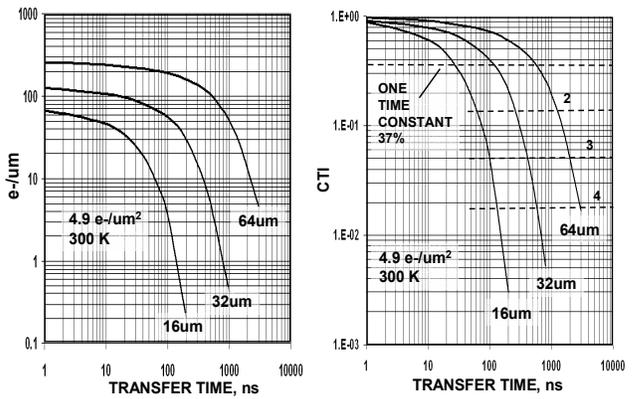
### 4.1 Photon transfer

The Mk x Nk pixel and related support circuitry have previously been incorporated, optimized and reported for various past fabricated CMOS imagers.<sup>4,6,7</sup> For example is the 3840 x 4096 x 10 um 5TPPD SoloHi imager shown in Fig. 13 is one such device. Figure 14 tabulates general performance parameters for the Mk x Nk imager where both PMOS and NMOS specifications are listed. Some characteristics can be elected by the user such as BSI or FSI. As we will discuss below CTE and full well depend on the PPD implants that can be also adjusted. Dark current and MTF performance depend on the silicon wafers used in fabricating the imager.

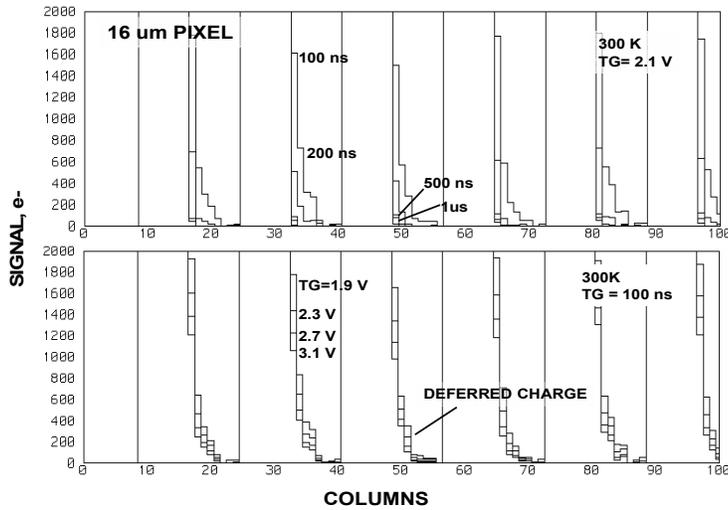
The full well capacity specified in Fig. 14 is dependent on the time needed to take an image including integration and readout time (which together we will call an 'exposure'). The dependence is due to charge jumping from the PPD over the TG barrier and into the SN by self induced and thermionic emission processes during an exposure.<sup>5</sup> Figure 15a theoretically plots charge capacity as a function of time over 32 orders of magnitude for various PPD potentials at room temperature. The model assumes that light is instantaneously (impulse) introduced to the PPD region at the beginning of an exposure. Note shorter exposures will exhibit greater full well performance than longer ones. Figure 15b is a similar plot but at a lower operating temperature (173 K, -100 C). Note that charge capacity improves compared to room temperature operation because electrons have less thermal energy to jump the TG barrier. SoloHi data is also included in Fig. 15a to demonstrate that thermionic effect just described tracks theory.



Figs. 7a,b. PISCES CTI with transfer time and signal density.



Figs. 8a,b. PISCES CTE with transfer time and pixel size.



Figs. 9a,b. CTE as function of TG clock width time and amplitude.

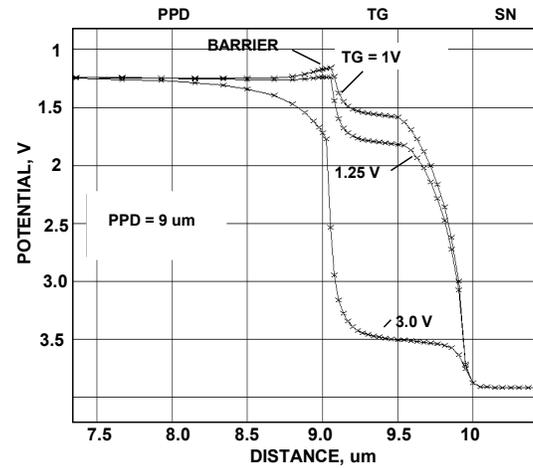


Fig. 10. PISCES potentials for the PPD, TG and SN regions.

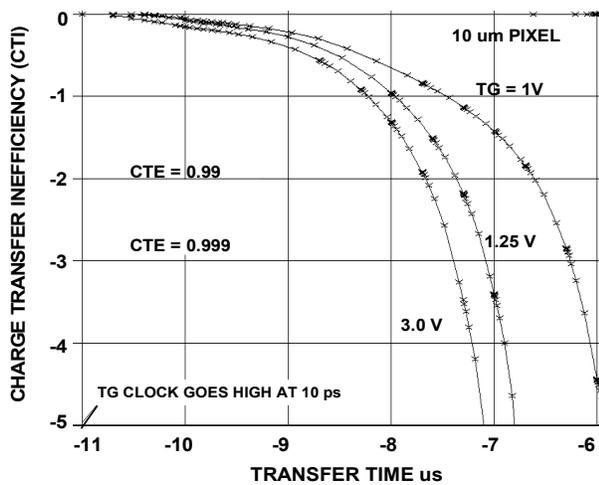


Fig. 11. CTI with transfer time and TG clock amplitude.

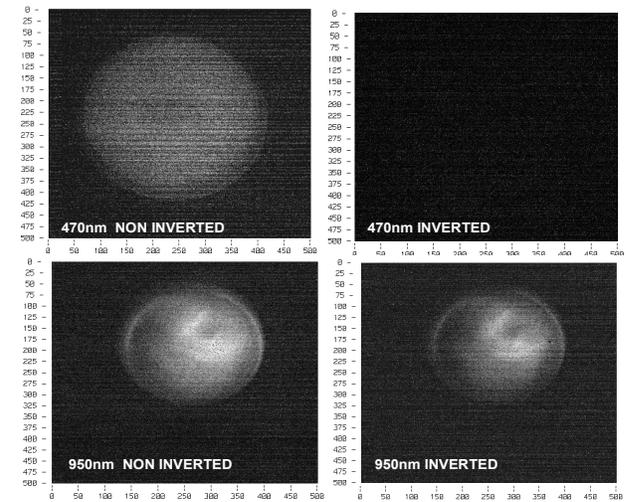


Fig. 12. TG trapping and residual bulk image (RBI) at two wavelengths.

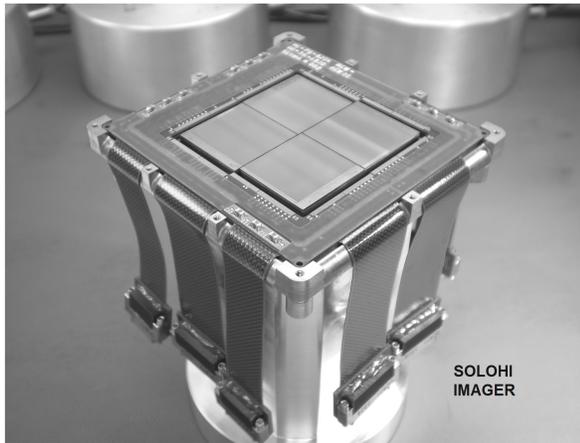
Figure 16 presents a photon transfer curve (PTC)<sup>8</sup> generated for a recently fabricated 496 x 512 x 10um 5TPPD pixel imager. Off chip CDS processing is utilized by using the raw signal output channel. The two MIM gain states characterized when combined yield an overall dynamic range of 10,000 (100 dB). Figures 17 and 18 present PTCs generated from the 1024 x 1024 x 16 um 6TPPD pixel sensor utilizing on-chip CDS processing with and without bandwidth control activated (via  $BW\_clk$ ). For the high MIM gain state (MIM off) the read noise is reduced from 4 e- to 2.8 e- when the video time constant,  $\tau_D$ , is increased from 500 ns to 5 us. Figures 19 and 20 shows the composition of noise floor for the same time constants. The top traces were taken under normal clocked reset conditions whereas the bottom traces show the noise floor when the reset clock is always 'on'. This action forces the SN to  $V_{REF}$  and in turn eliminates any noise sources up stream from the SN (e.g., dark current). Both background noise and random telegraph noise (RTN) are lowered when bandwidth is reduced (most notably the RTN that is within the band pass of the CDS).

#### 4.2 Charge transfer efficiency

Figure 21 shows what we refer to as the CTE 'square-wave response (SWR)' generated by an updated 5TPPD 10 um SoloHi pixel. SWR data is typically generated for a single row of pixels at a constant or changing signal level. We vary signal to measure CTE as a function of signal. CDS is first fully applied to the first pixel in the row (i.e., reset, clamp, transfer, sample, ADC encode) before moving onto the next pixel and repeating the same routine for other pixels contained in the row. As pixels are processed in this manner a LED light source is switched 'on' and 'off' illuminating the entire array of pixels. Image lag (or deferred charge) is measured immediately after the LED light goes 'off'. Trailing charge (first trailer, second trailer, etc.) represents a measurement of image lag. Signal charge is captured after the LED light source is turned 'on.' Depending on the emission time constant and severity of the CTE problem most deferred charge can be accounted for with 8 pixels after the LED shuts off in CTE data presented below. If not, the number of pixels following LED off condition can be increased. Summing deferred charge contained within the 8 columns gives us an estimate for CTE performance using the simple equation  $CTE = 1 - Q_{DEF} / S_T$  where  $Q_{DEF}$  is the net deferred charge measured and  $S_T$  is the test signal level. Figure 21 shows the increase in deferred charge with signal especially for the first trailer after the LED light is turned off. Both high and low MIM gain states are shown. The CTE improves for the low gain state because the voltage on the SN is higher producing larger fringing field between PPD and SN resulting in less trapping.

Figure 22 presents CTE performance as a function of signal for a 10 um 5TPPD imager. The CTE is derived from Fig. 21. The CTE reduction observed with signal is related to a decrease in the fringing field strength between the PPD and SN. The decrease slows the transfer process which in turn promotes more TG trapping. Also, as the SN potential collapses charge has more of an opportunity to thermally jump from the SN back into the TG resulting in even more trapping. At some signal level the TG and SN potentials become equal at which point maximum trapping is observed. Figure 23 is an illustration of the PPD/TG/ SN regions and related potentials showing how this takes place. Figure 24 plots signal and net deferred charge contained in all 8 trailing dark pixels as a function of column number. Note that deferred charge gradually rises until column 320 is reached at which point the SN and TG potentials become equal where charge sharing takes place. Increasing TG drive lowers the 'charge share breakpoint' giving good reason to not overdrive the TG. Read noise also increases when TG and the SN share charge. This problem is seen in Fig. 25 where both deferred charge and noise are measured after a LED is turned off. Note that the true read noise of 2 e- is not obtained even after 120 TG cycles.

Inversion is an important bias condition necessary to manage TG dark current (refer to Sec. 4.3) and control PPD charge capacity. Inversion encourages holes provided by the substrate to collect at the surface of the TG. This happens when the TG barrier voltage is biased slightly negative relative to substrate potential. The holes electrically passivate interface states and recombine with charge trapped under the TG. This TG bias scheme is necessary for high speed erasure to assure that the PPD and TG don't contain charge before an image is captured. Figure 26 demonstrates how effective inversion is in eliminating trapped charge. However, signal loss can also occur because some holes remain trapped instead of returning quickly back to the substrate before charge transfer takes place (hole detrapping takes several microsecs). The trapped holes recombine with some of the signal electrons during transfer. It is therefore important to keep in mind that an absolute amount of charge is lost during the transfer process either by trapped charge making its way to the SN instead of the PPD, deferring charge from the target pixel or through TG recombination. The only means to an absolute CTE measurement and the amount of charge that is lost is through Fe-55 x-ray stimulation.<sup>5</sup> CTE problems discussed above are typically only issues related to signal levels approaching or greater than full well ( i.e., a saturated  $M_k \times N_k$  image after nuclear implosion is an extreme case). For low light CTE performance is near perfect (and very

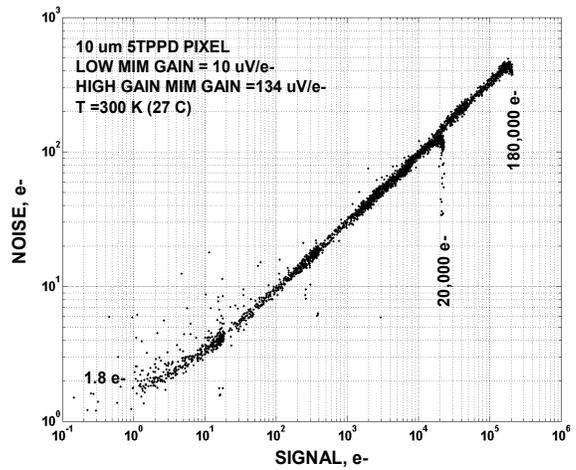
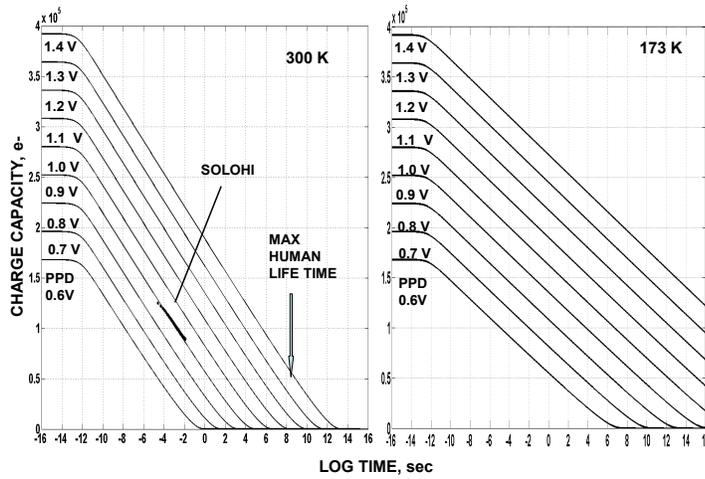


SPECTRAL PERFORMANCE (FSI)	NOMINAL VALUE
PIXEL FILL FACTOR	~ 50 %
QUANTUM EFFICIENCY	> 30 % avg 490-740 nm
SPECTRAL PERFORMANCE (BSI)	NOMINAL VALUE
PIXEL FILL FACTOR	100 %
QUANTUM EFFICIENCY	> 80 % avg 490-740 nm
CONVERSION GAIN (SENSE NODE)	NOMINAL VALUE
HIGH PIXEL GAIN	130 $\mu\text{V}/\text{e}-(\text{h}^+)$
LOW PIXEL GAIN	15 $\mu\text{V}/\text{e}-(\text{h}^+)$
RAW OUTPUT GAIN	NOMINAL VALUE
HIGH PIXEL GAIN	83 $\text{V}/\text{e}-(\text{h}^+)$
LOW PIXEL GAIN	9.6 $\mu\text{V}/\text{e}-(\text{h}^+)$
CDS OUT GAIN	NOMINAL VALUE
HIGH PIXEL GAIN	53 $\mu\text{V}/\text{e}-(\text{h}^+)$
LOW PIXEL GAIN	6.1 $\mu\text{V}/\text{e}-(\text{h}^+)$
FULL WELL CAPACITY	NOMINAL VALUE
HIGH PIXEL GAIN	~ 20,000 $\text{e}-(\text{h}^+)$
LOW PIXEL GAIN	~ 150,000 $\text{e}-(\text{h}^+)$
NON V/V LINEARITY	NOMINAL VALUE
HIGH PIXEL GAIN	< 4% < 18,000 $\text{e}-(\text{h}^+)$
LOW PIXEL GAIN	< 4% < 150,000 $\text{e}-(\text{h}^+)$

READ NOISE (RAW CHANNEL)	NOMINAL VALUE	
HIGH PIXEL GAIN	1.5 $\text{h}^+$ rms	2.25 $\text{e}^-$ rms
LOW PIXEL GAIN	10 $\text{h}^+$ rms	15 $\text{e}^-$ rms
READ NOISE (CDS CHANNEL)	NOMINAL VALUE	
HIGH PIXEL GAIN	2 $\text{h}^+$ rms	3 $\text{e}^-$ rms
LOW PIXEL GAIN	13 $\text{h}^+$ rms	20 $\text{e}^-$ rms
DARK CURRENT (300 K)	NOMINAL VALUE	
NON INVERTED	2400 $\text{e}^-/\text{s}$	
INVERTED	400 $\text{e}^-/\text{s}$	
DARK CURRENT FPN (300 K)	NOMINAL VALUE	
NON INVERTED	5 %	
INVERTED	30 %	
OPTICAL FPN	NOMINAL VALUE	
PIXEL SF V/V FPN	~1 %	
CHARGE TRANSFER EFFICIENCY	NOMINAL VALUE	
MTF at 700 nm (Nyquist)	> 30 %	
IMAGE LAG	< 1 %	
POWER REQUIREMENTS	NOMINAL VALUE	
READOUT 16 fps, CDS OUTPUTS	< 90 mW	
INTEGRATING	< 20 mW	

Fig 13. NASA's SoloHi 3840(V) x 4096(H) x 10  $\mu\text{m}$  5TPPD imager.<sup>6,7</sup>

Fig 14.  $M_k \times N_k$  expected performance.



Figs. 15a,b. Charge capacity with time, PPD potential and temperature.

Fig.16. PTC for a 10  $\mu\text{m}$  5TPPD pixel array.

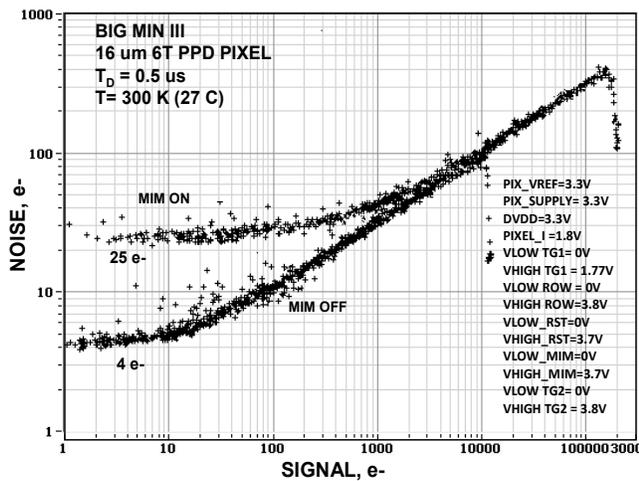


Fig. 17. PTC with CDS bandwidth open ( $\tau_D=0.5$  us).

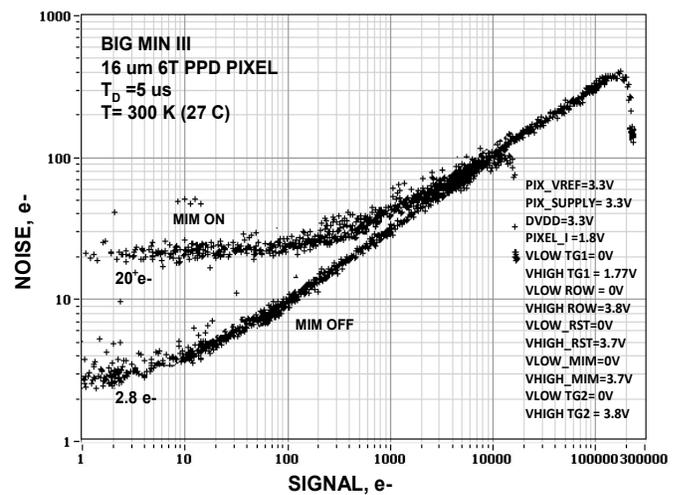


Fig. 18. PTC with reduced bandwidth with less read noise ( $\tau_D=5$  us).

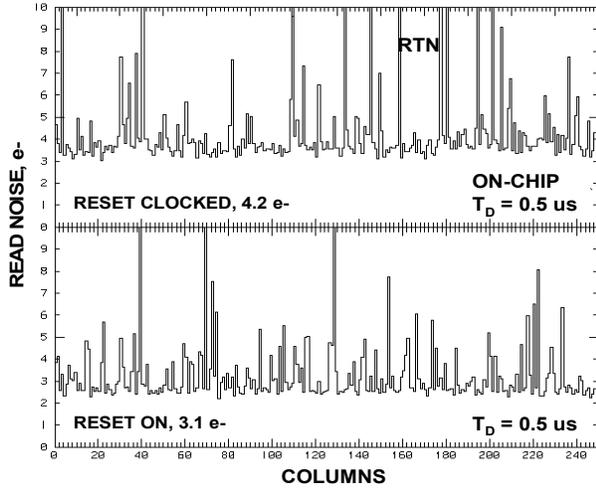


Fig. 19. Noise generated by pixels with bandwidth open ( $\tau_D=0.5\mu s$ ).

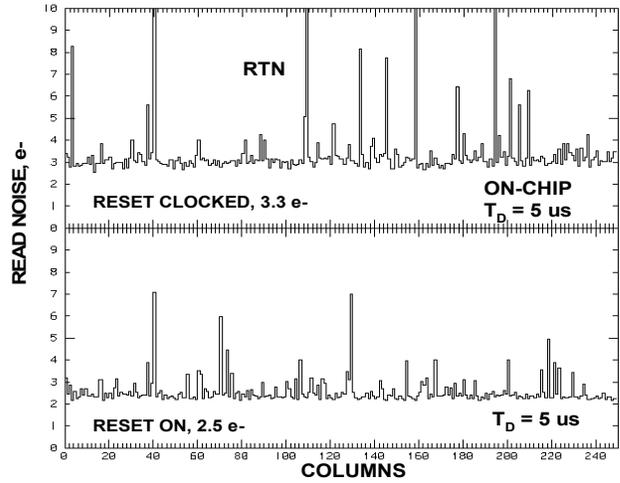
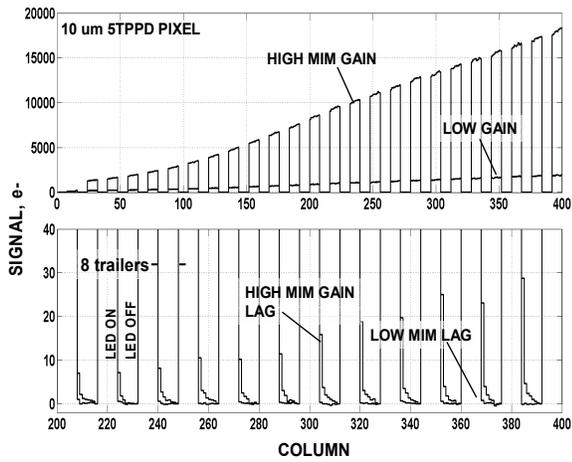


Fig. 20. Noise with reduced bandwidth ( $\tau_D=5\mu s$ ).



Figs. 21. Square wave CTE response showing deferred charge.

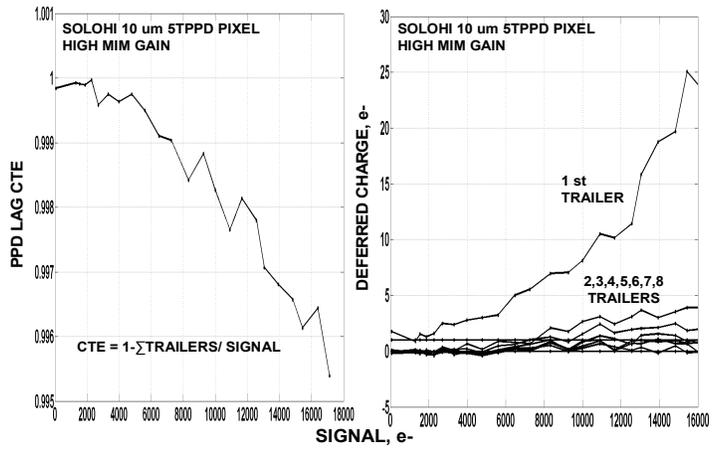


Fig. 22a,b. CTE and deferred charge trailers with signal.

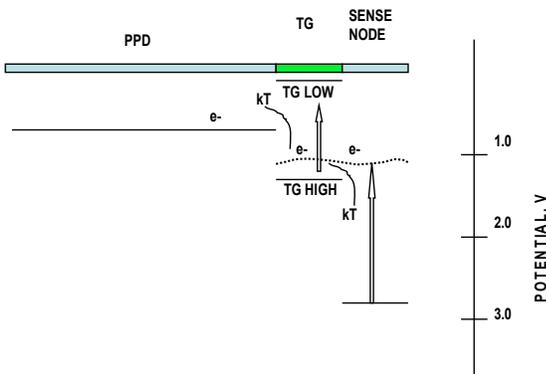


Fig. 23. PPD, TG and SN potentials during transfer.

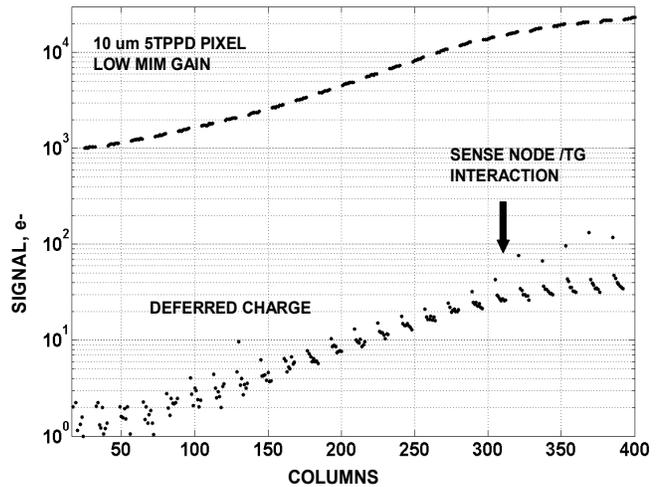


Fig. 24. Deferred charge increase when SN and TG potentials become equal.

difficult to measure !). Figure 27 shows a low light square wave-image for a 10  $\mu\text{m}$  5TPPD image. The upper left hand corner is only 8 e- p-p with a corresponding contrast signal-to-noise (S/N)  $\sim$  2.3. The lower right hand corner shows a 250 e- p-p level with a S/N= 16. Figure 28 presents a 3D image showing the distribution of charge levels across the 256 x 256 array investigated. Deferred and recombination loss is undetectable.

### 4.3 Dark current

The principal source of dark current is generated by the TG unless it is biased into inversion. Figure 29 and 30 present stacked row trace plots showing the dark FPN generated. The average dark current decreases from 2644 to 192 e-/sec when the TG is driven into inversion. Corresponding histograms are also presented in each figure. We expect to see a similar average dark current floor for the Mk x Nk since the same type of silicon wafers will be used. Note that the inverted state shows some hot pixels within the 256 x 256 region measured. Hot pixel density varies with chip location on the silicon wafer as well as wafer to wafer. The source of hot pixels may perhaps be related to the quality of silicon wafer (impurities, lattice defects) and/or impurity contamination of the wafer during fab. Figure 31 shows low light pictures taken from the BIG MIN III imager under noninverted and inverted conditions at  $\sim$ 35 C. The average signal level of the images is  $\sim$  200 e-. Dark FPN (primarily hot pixels) has been removed leaving only dark shot noise. Figure 32 shows histograms of each image. The S/N for the inverted image is clearly higher because of lower dark shot noise. Figure 33 is dark data taken from the 16  $\mu\text{m}$  6TPPD BIG MIN III array showing the effectiveness of inversion in reducing TG dark current.

Figure 34 presents a dark image generated by a BSI BIG MIN III array (shown packaged in Fig. 35). Average backside dark current is equal to FSI (400 e-/sec at 300K). We expect the BSI Mk x Nk imager will have identical dark current since the same thinning process will be used. However, there are a few isolated troubled regions found on the imager tested here. For example, the bright circular region at the bottom of the chip is related to a pixel substrate short that sometimes crops up during fab which generates luminescence. Also, the thinning process has left a narrow region of unthinned material on the right side on the imager. Along that border in the upper right hand there is an overly thinned region that generates dark current. The near IR response shown in Fig. 36 in the same region is lower than the rest of the array indicating that it may be in fact overly thinned. The narrow band 940 nm response is also used measure the uniformity of thinning by using interference fringes as a means to determine relative thickness (approximately 1 fringe = 1/7  $\mu\text{m}$ ).<sup>5</sup> The problems above have solutions and aren't normally observed. Figure 34 was presented to show that issues like this can surface from time to time.

## ACKNOWLEDGMENTS

The authors are appreciative of Richard Mann for the fabrication of our imagers at Jazz/Tower Semiconductor. Special thanks to Almus Kenter of Smithsonian Astrophysical Observatory for his continuation of the BIG MIN III project that has greatly assisted the Mk x Nk imager effort. We also express thanks to Mike Lesser of the University of Arizona for his collaboration on thinning. This work was performed under the auspices of the U.S. Department of Energy by LLNL under Contract DE-AC52-07NA27344, LLNL-CONF-657599.”

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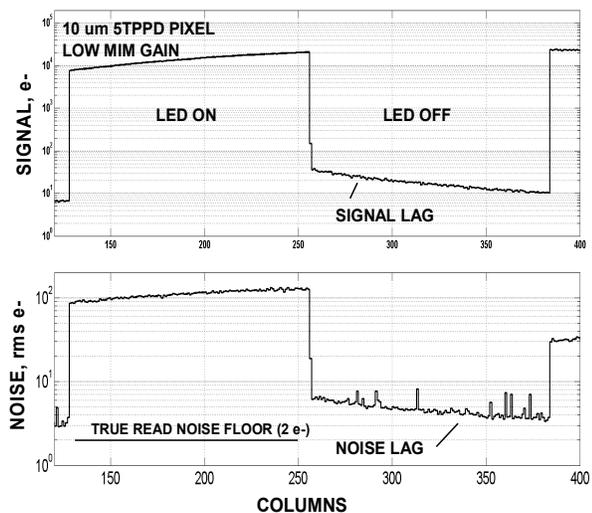


Fig. 25. Signal and noise lag.

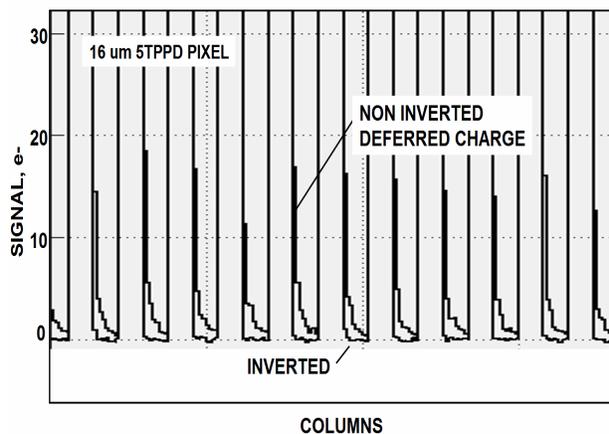


Fig. 26. Trapped charge elimination when TG is inverted.

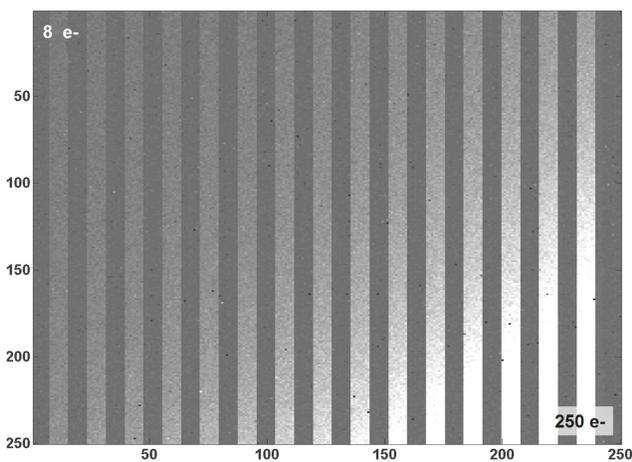


Fig. 27. Low light square-wave image.

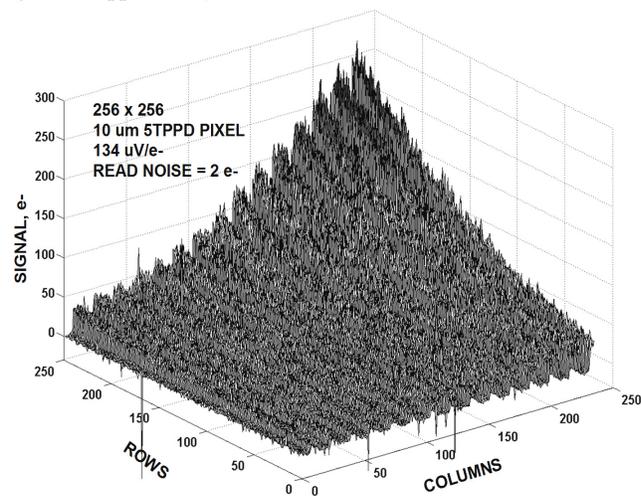


Fig. 28. Charge distribution for Fig. 27.

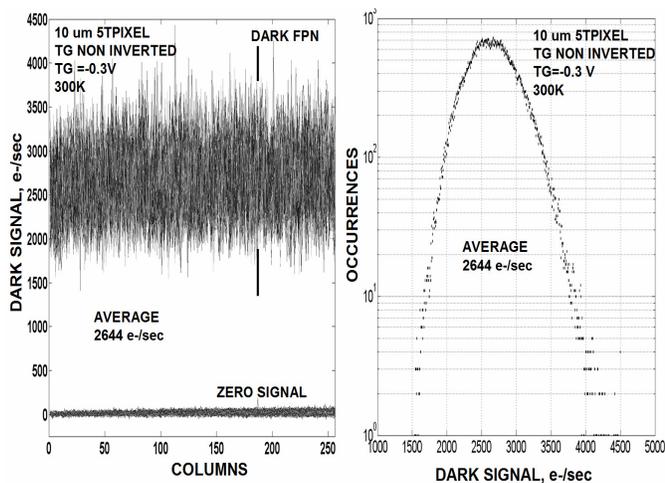


Fig. 29. Dark current under the non inverted condition.

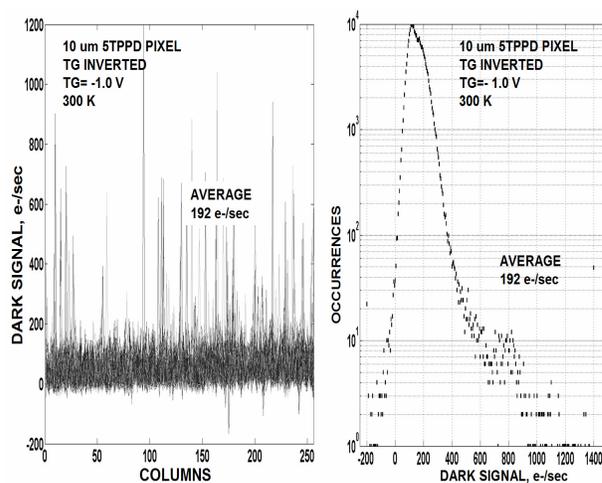


Fig. 30. Dark current under the inverted condition.



Fig. 31. Non inverted and inverted BIG MIN III images.

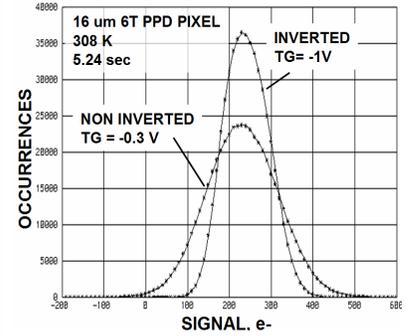


Fig. 32. Histograms for Fig. 31.

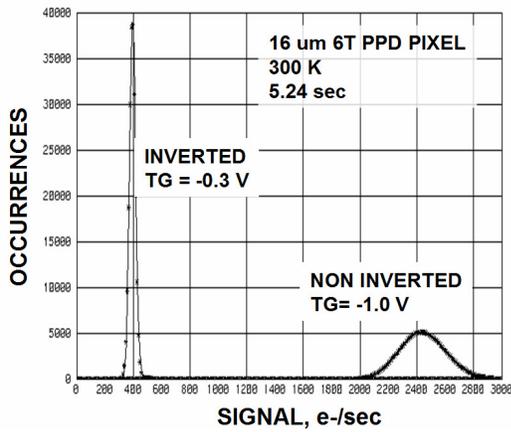


Fig. 33. Non inverted and inverted dark current histogram.

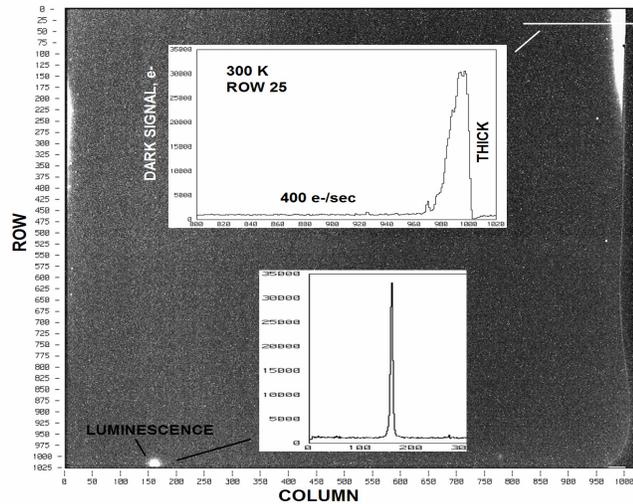


Fig. 34. Dark image for the BSI BIG MIN III imager.

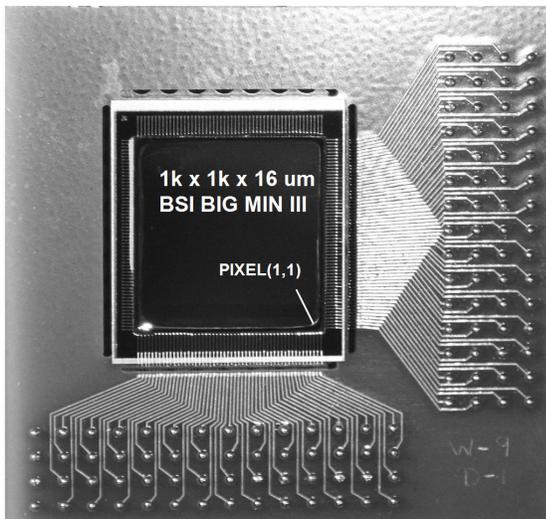


Fig. 35. A packaged BSI BIG MIN III imager.

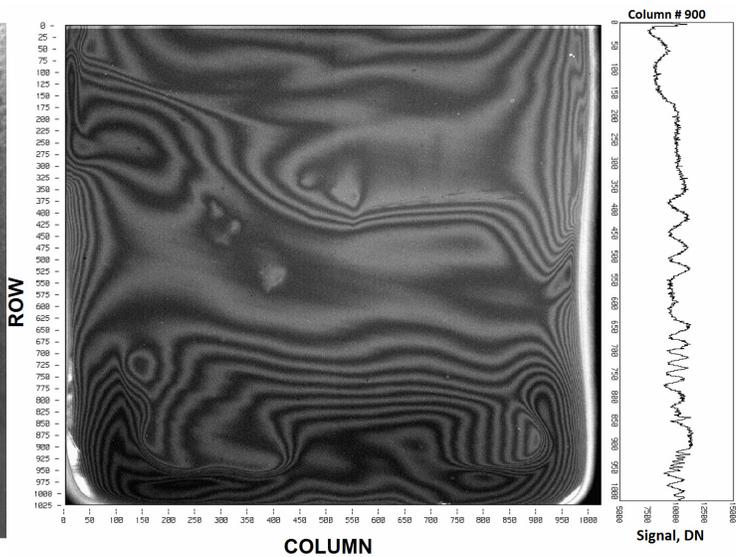


Fig. 36. 940 nm response showing interference fringing.